500mA, High PSRR, Low Dropout LDO

1 Features

- Input Voltage Range: 1.8V to 7.0V
- Output Current: 500mA
- Standard Fixed Output Voltage Options
  - 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 3.6V, 4.2V and 5.0V
- 40μA quiescent current
- <0.1μA shutdown current
- ±1.5% output voltage accuracy
- PSRR: 80dB@1KHz
- Dropout Voltage: 400mV@300mA, V_{OUT} = 3.3V
- Thermal shutdown protection
- Current limit protection
- RoHS Compliant and Halogen Free

2 Applications

- Portable Electric Devices
- Battery Powered Equipment
- Audio/Video Equipment

3 Description

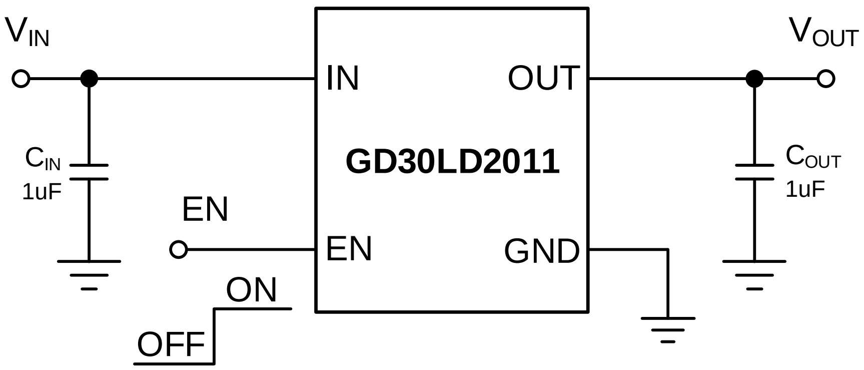
The GD30LD2011 is a high PSRR low dropout linear regulator with 500mA driving current. The GD30LD2011 shows good power dissipation with under 0.1μA shutdown current and 40μA quiescent current of light load for portable devices. The GD30LD2011 provides 1.2V to 5.0V output voltage for multiple application and it is with build-in thermal shutdown and current limit protection functions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE(NOM)
GD30LD2011	SOT23-5	2.92mm x 1.60mm
	DFN1x1-4	1.00mm x 1.00mm

1. For all available packages, see the *Package Information* and *Ordering Information* at the end of data sheet.

Simplified Application Schematic



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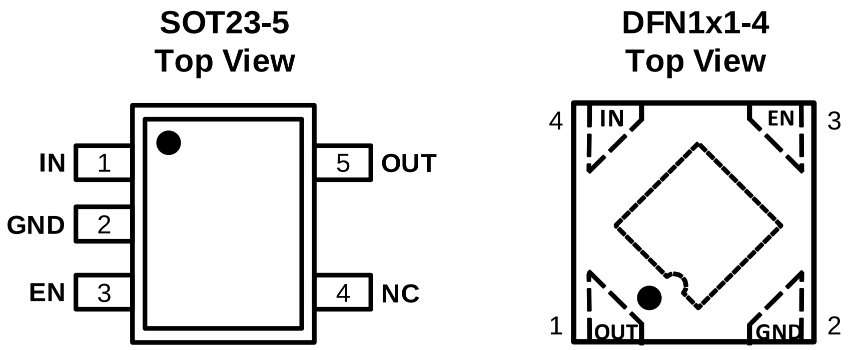
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PINS			PIN TYPE[1]	FUNCTION
NAME	SOT23-5	DFN1x1-4		
IN	1	4	P	Power supply input pin.
GND	2	2	G	Ground pin.
EN	3	3	I	Enable control pin. Active high.
NC	4			No connection.
OUT	5	1	P	Output pin.

1. I = Input, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	IN	−0.3	8	V
V_{EN}	EN	−0.3	8	V
V_{OUT}	OUT	−0.3	8	V
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−55	150	°C
PD	Power dissipation, SOT23-5 @ T_A = 25°C		0.4	W
	Power dissipation, DFN1x1-4 @ T_A = 25°C		0.4	

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	1.8		7	V
I_{OUT}	Output current	0		500	mA
T_J	Operating junction temperature[2]	−40		125	°C
T_A	Operating ambient temperature[2]	−40		85	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. In applications where high power dissipation and poor package thermal resistance is present, the maximum ambient temperature can need to be derated.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±200	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	SOT23-5	250	°C/W
		DFN1x1-4	250	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = V_{EN} = 5V, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage		1.8		7	V
V_{OUT}	Output voltage accuracy	V_{IN} = V_{OUT} +1V, I_{OUT} = 1mA	−1.5		+1.5	%
I_{OUT}	Output current		0		500	mA
I_Q	Quiescent current	V_{IN} = V_{EN} = 7V, no load		40	60	μA
I_{SHDN}	Shutdown current	V_{EN} = 0V		0.01	0.1	μA
V_{DO}	Dropout voltage[2]	V_{OUT} = 3.3V, I_{OUT} = 300mA		400		mV
		V_{OUT} = 2.8V, I_{OUT} = 300mA		450		
		V_{OUT} = 1.8V, I_{OUT} = 300mA		720		
		V_{OUT} = 1.2V, I_{OUT} = 300mA		980		
ΔLINE	Line regulation	V_{OUT} +1 ≤ V_{IN} ≤ 7V, I_{OUT} = 1mA			0.5	%
ΔLOAD	Load regulation	1mA ≤ I_{OUT} ≤ 500mA			2	%
V_{EN_RISE}	Rising enable threshold	EN input voltage high	1.5			V
V_{EN_FALL}	Falling enable threshold	EN input voltage low			0.4	V
PSRR	Power supply rejection ration	V_{IN} = V_{OUT} + 1V, I_{OUT} = 10mA, f = 100Hz		90		dB
		V_{IN} = V_{OUT} + 1V, I_{OUT} = 10mA, f = 1KHz		80		dB
		V_{IN} = V_{OUT} + 1V, I_{OUT} = 10mA, f = 10KHz		66		dB
R_{DIS}	Output discharge resistance			80		Ω
T_{TSD}	Thermal shutdown temperature[1]			155		°C
T_{HYS}	Thermal shutdown hysteresis[1]			20		°C

1. Guaranteed by design and engineering sample characterization.
2. The dropout voltage is defined as VIN – VOUT, when VOUT is 95% of the value of VOUT.

5.6 Typical Characteristics

V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 1.0μF, T_A = 25°C, unless otherwise noted.

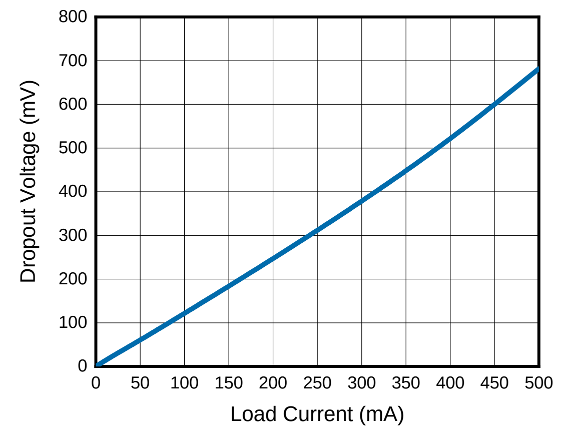


Figure 1. Dropout Voltage vs. Output Current

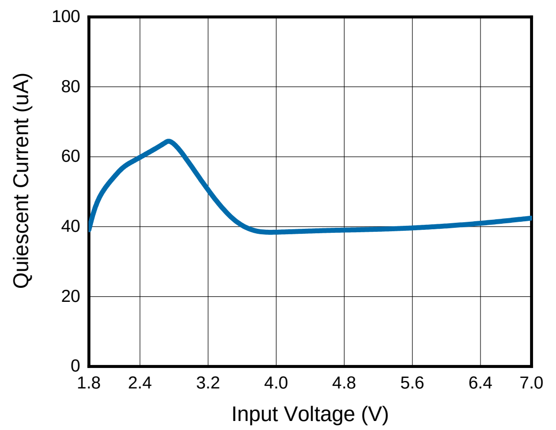


Figure 2. Quiescent Current vs. Input Voltage

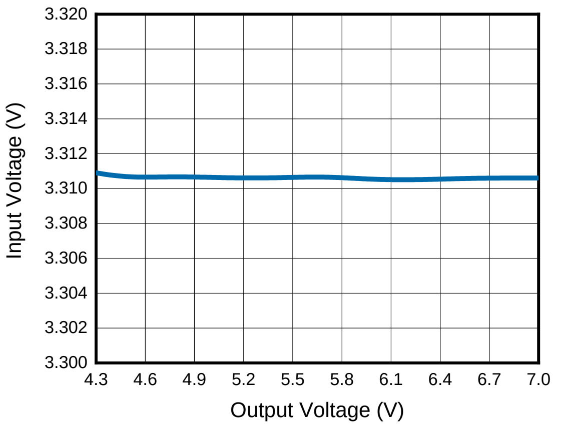


Figure 3. Output Voltage vs. Input Voltage

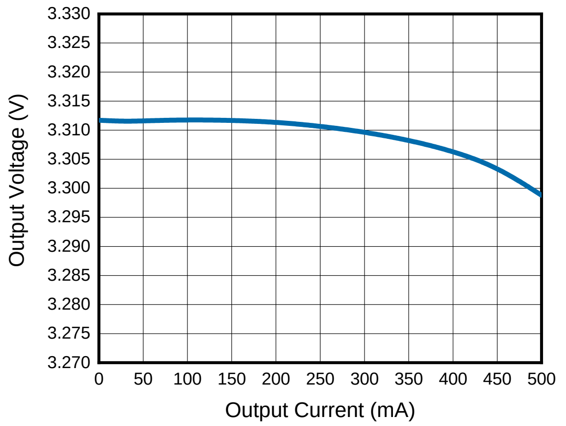


Figure 4.Output Voltage vs. Output Current

6 Functional Description

6.1 Block Diagram

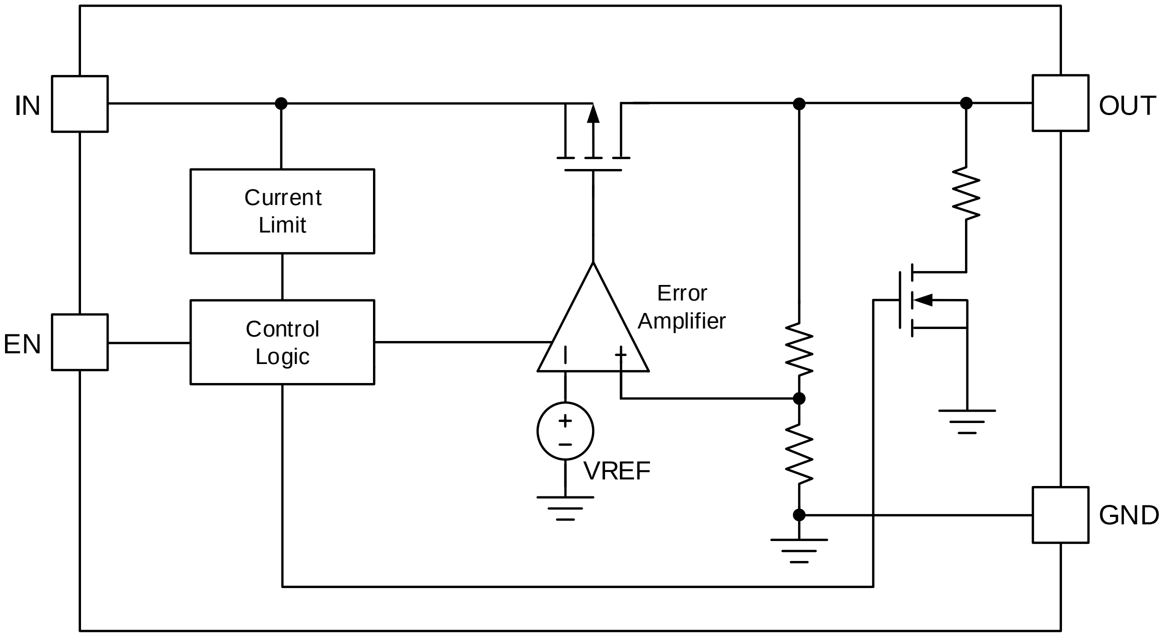


Figure 5. GD30LD2011 Functional Block Diagram

6.2 Operation

The external input and output capacitors of GD30LD2011 series must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the device IN and GND pins. The GD30LD2011 series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Place the output capacitor close to the device OUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

6.2.1 Dropout Voltage

The GD30LD2011 series use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout condition.

6.2.2 Current Limit Protection

The GD30LD2011 series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 650mA (typical). The output can be shorted to ground indefinitely without damaging the part.

6.2.3 Output Discharge Function

The GD30LD2011 series can discharge the output capacitor. When the V_{IN} ready and EN pin is in logic low, the internal NMOS between OUT and GND will be turned on. The discharge resistance (R_{DIS}) is 80Ω).

6.2.4 Thermal Shutdown

The over temperature protection function of GD30LD2011 series will turn off the P-MOSFET when the junction temperature exceeds 150°C (typical). Once the junction temperature cools down by approximately 20°C, the regulator will automatically resume operation.

6.3 Device Mode Description

6.3.1 Device Enable

The GD30LD2011 series has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. When the EN pin is in logic low, the shutdown current is almost 0.1μA typical. The EN pin may be directly tied to IN to keep the part on.

7 Application Information

The GD30LD2011 is high voltage, low power consumption and low dropout LDO. Its output voltage is fixed, providing two versions with or without enable.

7.1 Typical Application Circuit

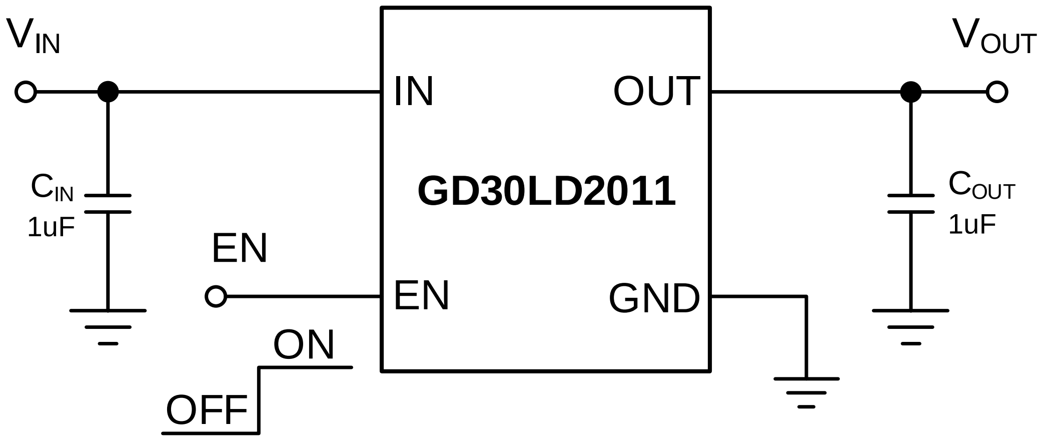


Figure 6. Reference Design Schematic

7.2 Detailed Design Description

7.2.1 Input Capacitor Selection

A 1μF or lager ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

7.2.2 Output Capacitor Selection

The GD30LD2011 series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. A 1μF or lager ceramic capacitor(dielectric types X5R or X7R) place as close as to the IC's OUT and GND pins. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Increasing capacitance and decreasing ESR can also improve the circuit's PSRR and line transient response.

7.3 Power Dissipation

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (1)$$

$V_{IN} \times V_{OUT}$ represents the static power consumption of the LDO, the value is relatively small and can be ignored. An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

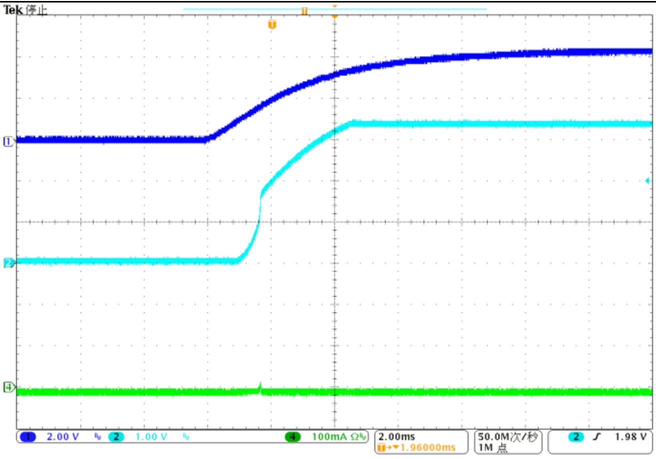
The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB, device package, and the temperature of the ambient air (T_A). The maximum power dissipation can be calculated as below:

$$T_J = T_A + \theta_{JA} \times P_D \tag{2}$$

$$I_{OUT} = \frac{T_J - T_A}{\theta_{JA} \times (V_{IN} - V_{OUT})} \tag{3}$$

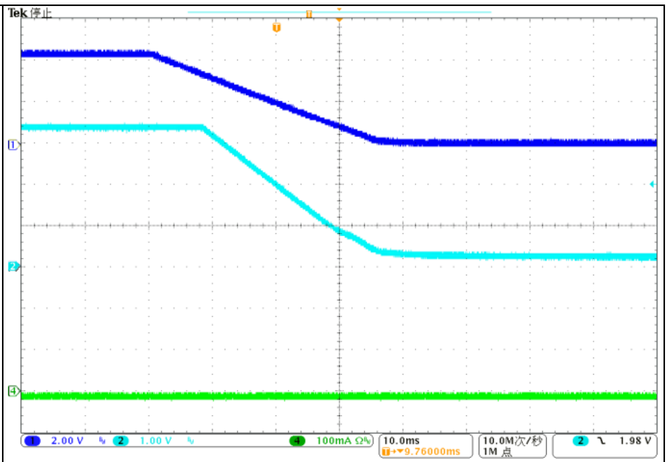
7.4 Typical Application Curves

V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.



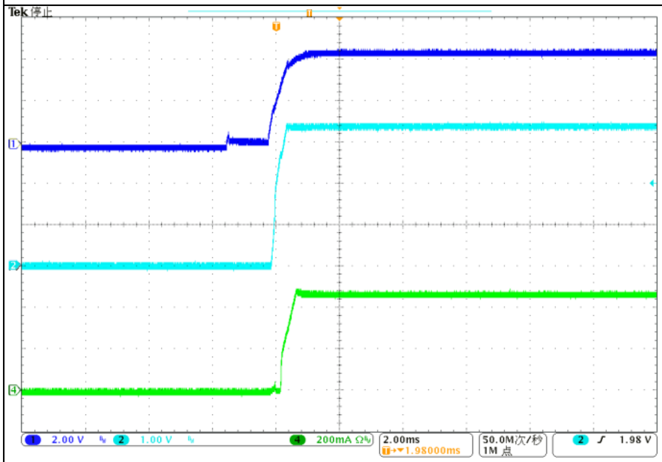
CH1=V_{IN}, CH2=V_{OUT}, CH3=I_{OUT}, I_{OUT} = 0A

Figure 7. VIN Startup without Load



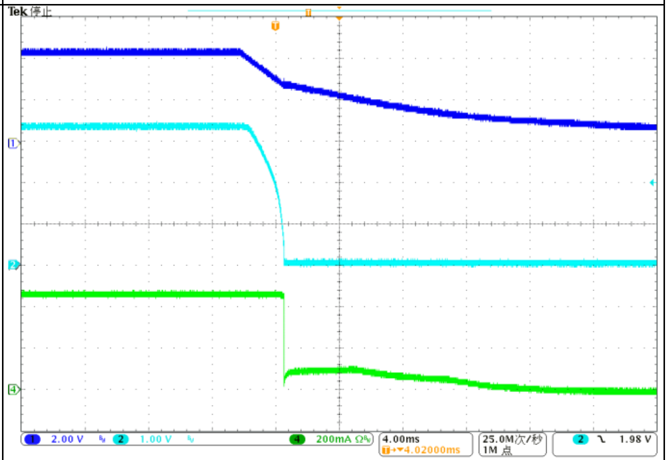
CH1=V_{IN}, CH2=V_{OUT}, CH3=I_{OUT}, I_{OUT} = 0A

Figure 8. VIN Shutdown without Load



CH1=V_{IN}, CH2=V_{OUT}, CH3=I_{OUT}, I_{OUT} = 0.5A

Figure 9. VIN Startup with Load

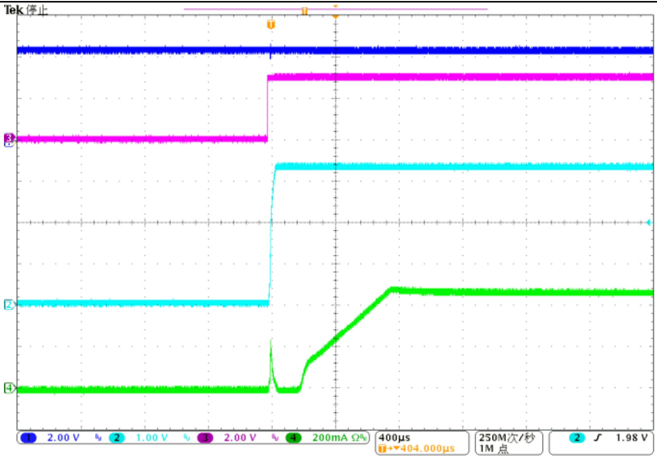


CH1=V_{IN}, CH2=V_{OUT}, CH3=I_{OUT}, I_{OUT} = 0.5A

Figure 10. VIN Shutdown with Load

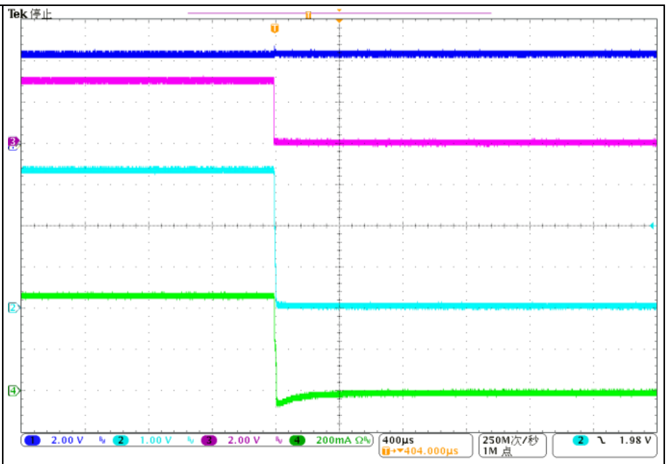
Typical Application Curves(Continued)

V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise noted.



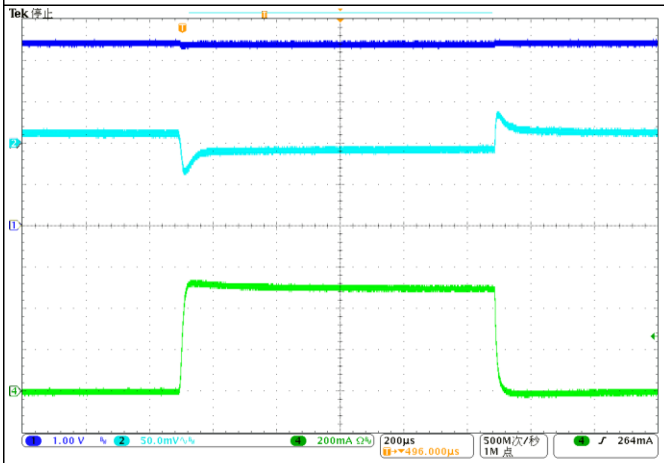
CH1=V_{EN}, CH2=V_{OUT}, CH3=I_{OUT}, I_{OUT} = 0.5A

Figure 11. EN Startup with Load



CH1=V_{EN}, CH2=V_{OUT}, CH3=I_{OUT}, I_{OUT} = 0.5A

Figure 12. EN Shutdown with Load



CH1=V_{IN}, CH2=V_{OUT}/AC, CH3=I_{OUT}, I_{OUT} = 0A to 0.5A

Figure 13. Load Transient

8 Layout Guidelines and Example

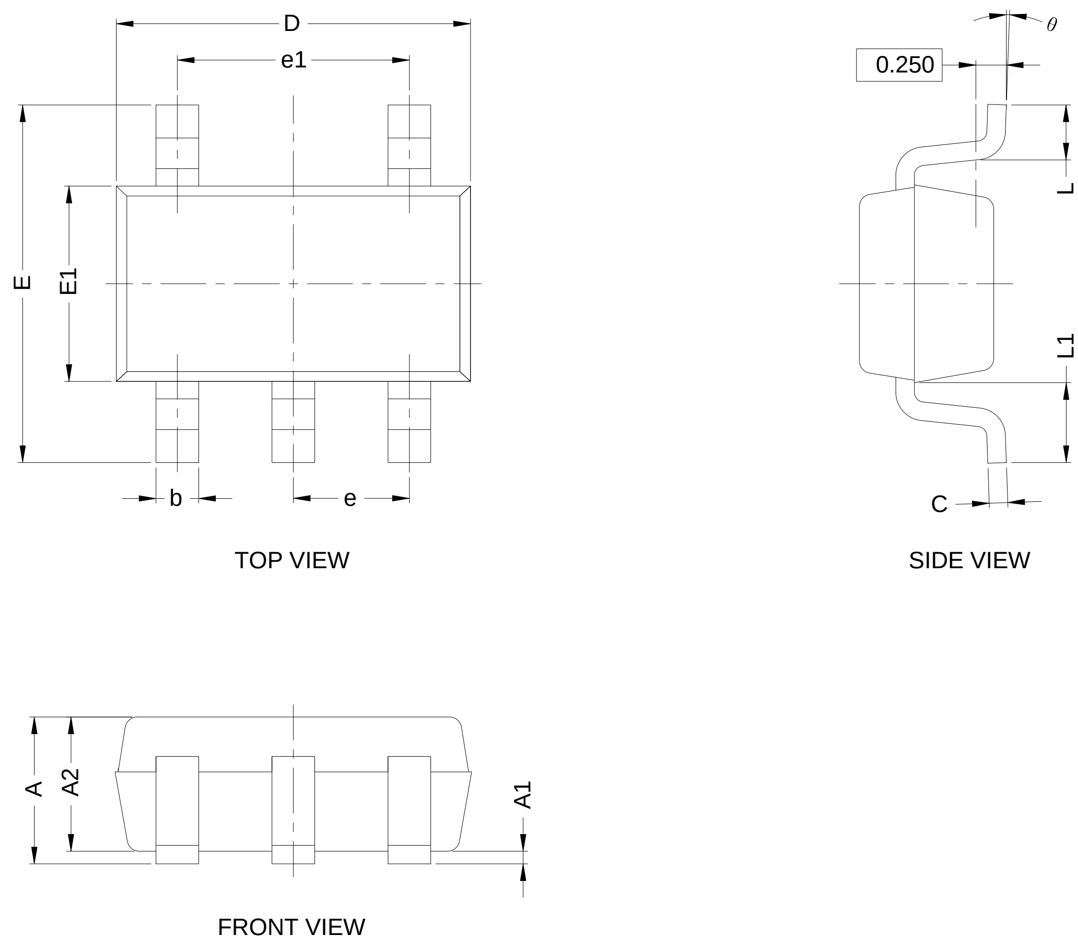
By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the GD30LD2011 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

9 Package Information

9.1 Outline Dimensions

SOT23-5 Package Outline



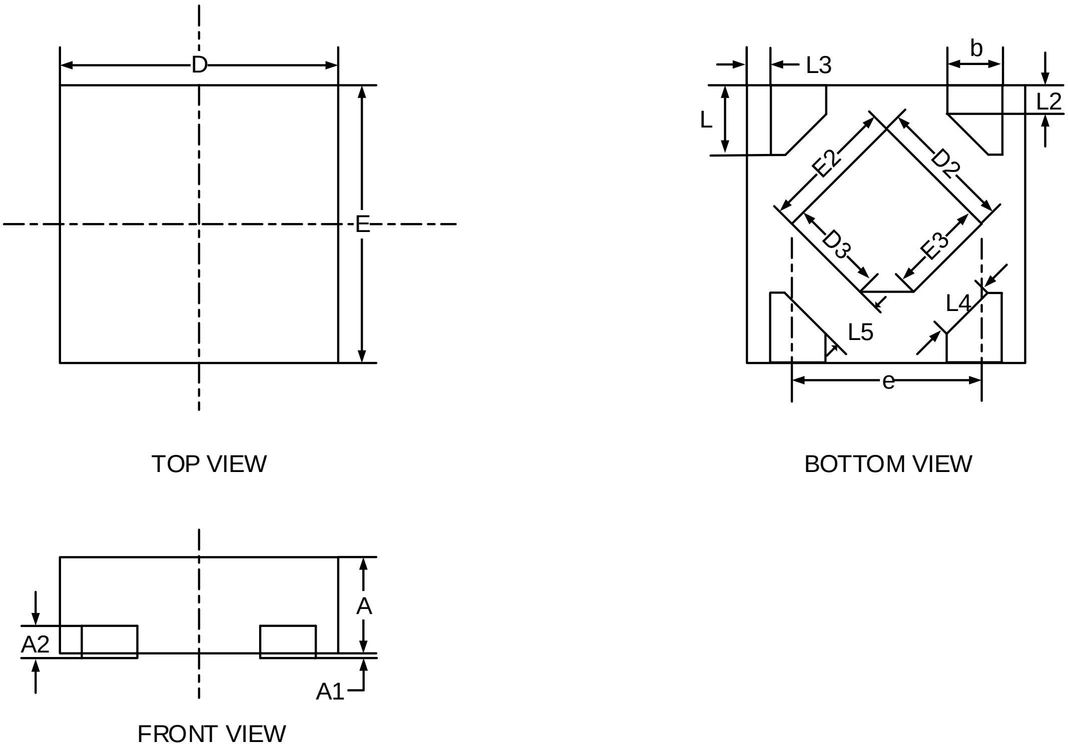
NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 1 *SOT23-5 dimensions(mm)*.

Table 1. SOT23-5 dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	1.05		1.25
A1	0.00		0.10
A2	1.05	1.10	1.15
b	0.30		0.50
c	0.10		0.20
D	2.82	2.92	3.02
E	2.65		2.95
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.60
L1	0.60 REF		
θ	0°		8°

DFN1x1-4 Package Outline



NOTES: (continued)

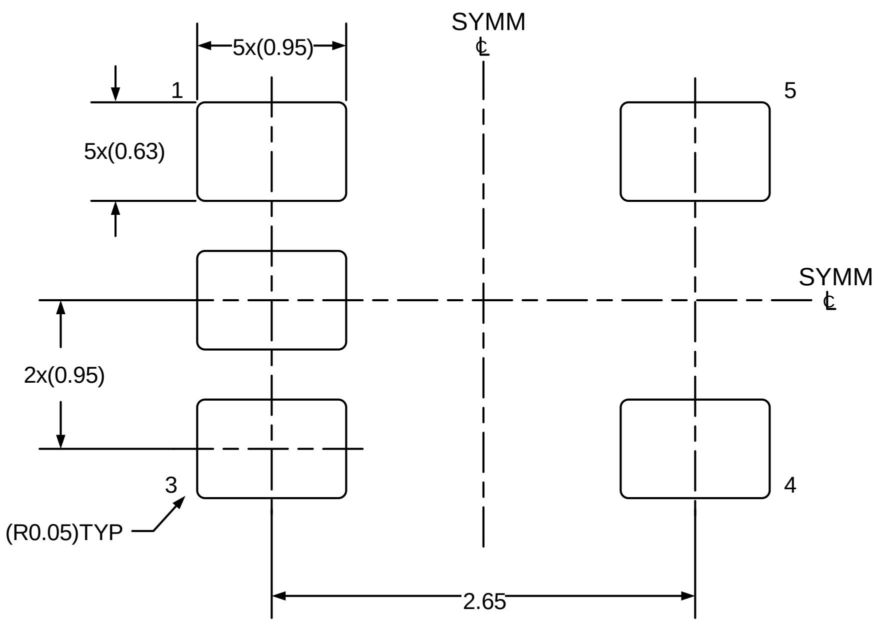
1. Refer to the Table 2 *DFN1x1-4 dimensions(mm)*.

Table 2. DFN1x1-4 dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.35		0.40
A1	0.00	0.02	0.05
A2	0.127REF		
b	0.15	0.20	0.25
D	0.95	1.00	1.05
D2	0.38	0.48	0.58
D3	0.230	0.330	0.430
E	0.95	1.00	1.05
e	0.65BSC		
E2	0.38	0.48	0.58
E3	0.230	0.330	0.430
L	0.20	0.25	0.30
L2	0.103REF		
L3	0.075REF		
L4	0.208REF		
L5	0.200 REF		

9.2 Recommended Land Pattern

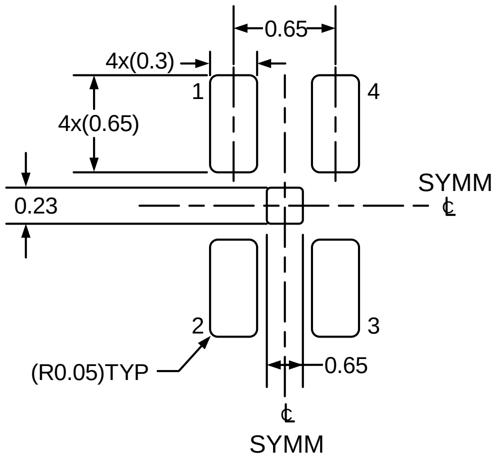
SOT23-5 Land Pattern Example



NOTES:

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

DFN1x1-4 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30LD2011NSTR-I12	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I15	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I18	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I25	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I28	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I30	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I33	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I36	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I42	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011NSTR-I50	SOT23-5	Green	Tape & Reel	3000	−40°C to +125°C
GD30LD2011JETR-I12	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I15	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I18	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I25	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I28	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I30	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I33	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I36	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I42	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C
GD30LD2011JETR-I50	DFN1x1-4	Green	Tape & Reel	10000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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