

General-Purpose, Micro-Power 1.2MHz, RRIO Precision Amplifiers

1 Features

- Precision: 2.5mV Maximum Positive Input Offset Voltage
- Low Noise: 30nV/√Hz at 1kHz
- 1.2MHz GBW for Unity-Gain Stable
- Micro-Power: Total 375μA Supply Current
- Single 1.8V to 5.5V Supply Voltage Range at 0°C to 70°C
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Extended Temperature Range: -40°C to +125°C

2 Applications

- Battery-Powered Instruments:
 - Consumer, Industrial, Medical, Notebooks
- Audio Outputs
- Wireless Chargers
- Sensor Signal Conditioning:
 - Sensor Interfaces, Loop-Powered, Active Filters
- Wireless Sensors:
 - Home Security, Remote Sensing, Wireless Metering

3 Description

The GD30AP324H of quad-channel amplifiers provides input offset voltage correction for positive low offset (2.5mV maximum) and drift (1μV/°C)

through the use of proprietary techniques. Featuring rail-to-rail input and output swings, and low quiescent current (total 375μA typically) combined with a wide bandwidth of 1.2MHz and low noise (30nV/√Hz at 1kHz) makes this family very attractive for a variety of battery-powered applications such as handsets, tablets, notebooks, and portable medical devices. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the GD30AP324H amplifiers provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 500pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection (5kV HBM). The GD30AP324H amplifiers are optimized for operation at voltages as low as +1.8V (±0.9V) and up to +5.5V (±2.75V) at the temperature range of 0°C to 70°C, and operation at voltages from +2.0V (±1.0V) to +5.5V (±2.75V) over the extended temperature range of -40°C to +125°C.

The quad-channel GD30AP324H is offered in both SOIC-14L and TSSOP-14L packages.

Device Information¹

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AP324H	SOIC-14L	8.73mm x 3.95mm
	TSSOP-14L	4.96mm x 4.40mm

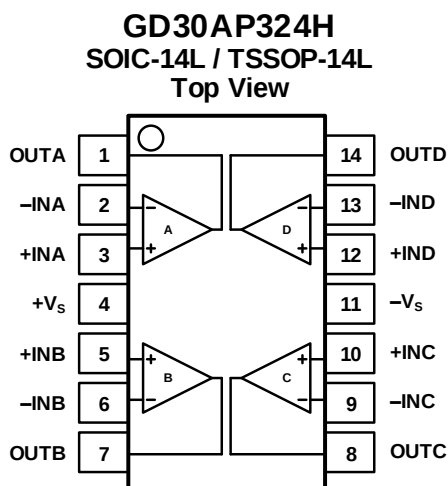
1. For all available packages, see the [Package Information](#) and [Ordering Information](#) at the end of data sheet.

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4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

NAME	PIN TYPE ¹	FUNCTION
-IN	I	Inverting input of the amplifier. The voltage range is from ($V_{S-} - 0.1V$) to ($V_{S+} + 0.1V$).
+IN	I	Non-inverting input of the amplifier. This pin has the same voltage range as -IN.
+Vs	P	Positive power supply. The voltage is from 2.0V to 5.5V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 2.0V to 5.5V.
-Vs	P	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 2.0V to 5.5V.
OUT	O	Amplifier output.

1. I = Input, O = Output, P = Power.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)¹

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{S+} to V_{S-}	Supply Voltage		10.0	V
V_I	Signal Input Voltage	$V_{S-} - 0.3$	$V_{S+} + 0.3$	V
I_I	Signal Input Current	-10	10	mA
	Output Short-Circuit		Continuous	s
T_J	Junction Temperature, T_J		150	°C
T_{stg}	Storage Temperature Range, T_{stg}	-65	+150	°C
	Lead Temperature Range (Soldering 10 sec)		260	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL ^{1,2}	PARAMETER	MIN	TYP	MAX	UNIT
V_{S-} to V_{S+}	Input supply voltage range($T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)	1.8		5.5	V
	Input supply voltage range($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$)	2.0		5.5	V
V_{CM}	Common-mode voltage range	$V_{S-} - 0.1$		$V_{S+} + 0.1$	V
T_A	Operating temperature range	-40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017 ¹	±5000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022 ²	±2000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Characteristics

SYMBOL ¹	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	TSSOP-14L	112	°C/W
		SOIC-14L	115	

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

$V_S = 5.0\text{ V}$, $V_{CM} = V_S / 2$, $V_O = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $T_A = +25^\circ\text{C}$, unless otherwise noted. Boldface limits apply over the specified temperature range, $T_A = -40$ to $+125^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage		0		+2.5	mV
dV _{OS} /dT	Offset voltage drift ¹	T _A = −40 to +125°C		±1	+3	μV/°C
PSRR	Power supply rejection ratio	V _S = 2.0 to 5.5 V, V _{CM} < V _{S+} − 2V	80	106		dB
		T _A = −40 to +125°C	75			
INPUT BIAS CURRENT						
I _B	Input bias current ¹			1		pA
		T _A = +85°C		150		
		T _A = +125°C		500		
I _{OS}	Input offset current ¹			1		pA
NOISE						
V _n	Input voltage noise	f = 0.1 to 10 Hz		6		μV _{P-P}
e _n	Input voltage noise density	f = 10 KHz		27		nV/√Hz
		f = 1 KHz		30		
I _n	Input current noise density	f = 1 KHz		10		fA/√Hz
INPUT VOLTAGE						
V _{CM}	Common-mode voltage range		V _{S−} − 0.1		V _{S−} + 0.1	V
CMRR	Common-mode rejection ratio	V _S = 5.5 V, V _{CM} = −0.1 to 5.6 V	80	94		dB
		V _{CM} = 0 to 5.3 V, T _A = −40 to +125°C	72			
		V _S = 2.0 V, V _{CM} = −0.1 to 2.1 V	74	86		
		V _{CM} = 0 to 1.8 V, T _A = −40 to +125°C	66			
INPUT IMPEDANCE						
C _{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
A _{VOL}	Open-loop voltage gain	R _L = 10 kΩ, V _O = 0.05 to 3.5 V	90	105		dB
		T _A = −40 to +125°C	85			
		R _L = 600Ω, V _O = 0.15 to 3.5 V	85	100		
		T _A = −40 to +125°C	80			

Electrical Characteristics

$V_S = 5.0\text{ V}$, $V_{CM} = V_S / 2$, $V_O = V_S / 2$, and $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $T_A = +25^\circ\text{C}$, unless otherwise noted. Boldface limits apply over the specified temperature range, $T_A = -40$ to $+125^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain band width product			1.2		MHz
SR	Slew rate	G = +1, C _L = 100pF, V _O = 1.5 to 3.5 V		1		V/μs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 KHz, V _O = 0.5 V _{RMS}		0.0003		%
t _s	Settling time	To 0.1%, G = +1, 1V step		1.5		μs
		To 0.01%, G = +1, 1V step		1.8		
t _{OR}	Overload recovery time	V _{IN} * Gain > V _S		2.5		μs
OUTPUT						
V _{OH}	High output voltage swing	R _L = 10 kΩ		V _{S+} − 6	V _{S+} − 3	mV
		R _L = 600Ω		V _{S+} − 100	V _{S+} − 65	
V _{OL}	Low output voltage swing	R _L = 10 kΩ		V _{S−} + 2	V _{S−} + 4	mV
		R _L = 600Ω		V _{S−} + 42	V _{S−} + 65	
I _{SC}	Short-circuit current	Source current through 10Ω		45		mA
		Sink current through 10Ω		55		
POWER SUPPLY						
V _S	Operating supply voltage	T _A = 0°C to +70°C		1.8	5.5	V
		T _A = −40°C to +125°C		2.0	5.5	
I _Q	Quiescent current			375	490	μA

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

$V_{CM} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S/2$, at $T_A = +25^\circ C$, unless otherwise noted.

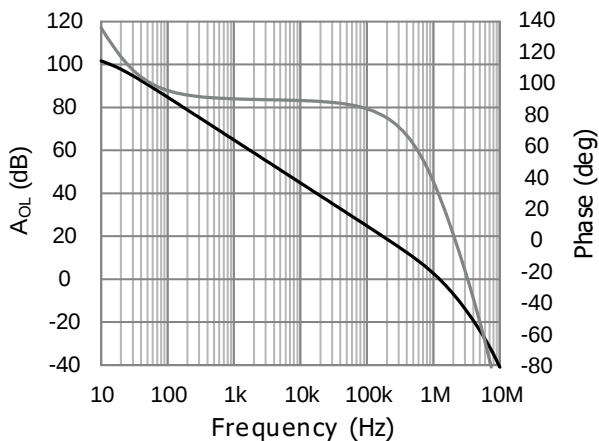


Figure 1. Open Loop Gain and Phase vs. Frequency

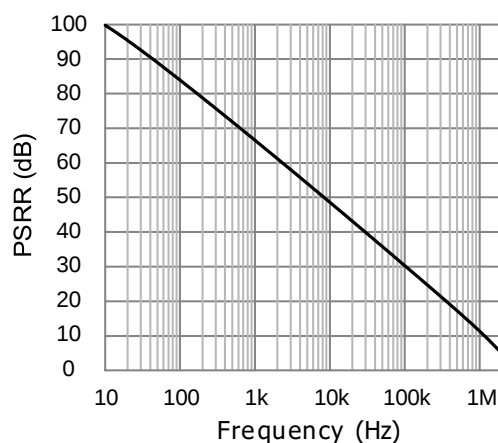


Figure 2. Power Supply Rejection Ratio vs. Frequency

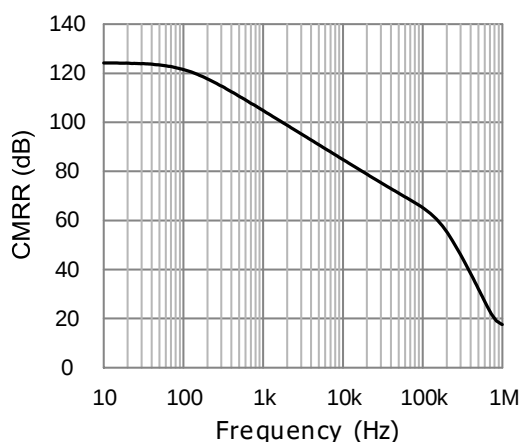


Figure 3. Common-mode Rejection Ratio vs. Frequency

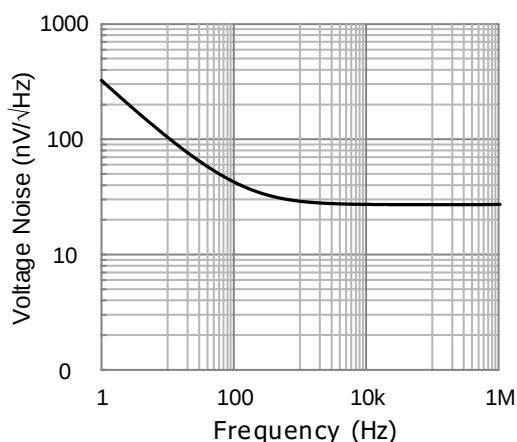


Figure 4. Input Voltage Noise Spectral Density vs. Frequency

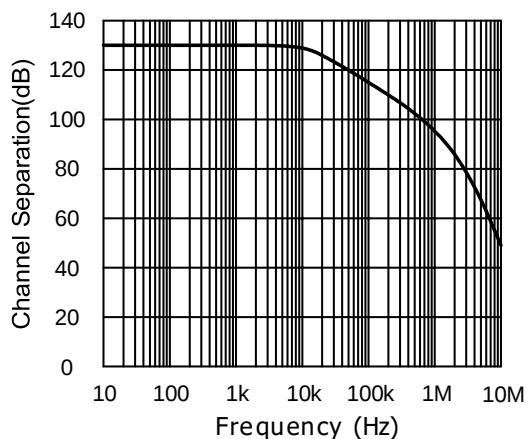


Figure 5. Channel Separation vs. Frequency

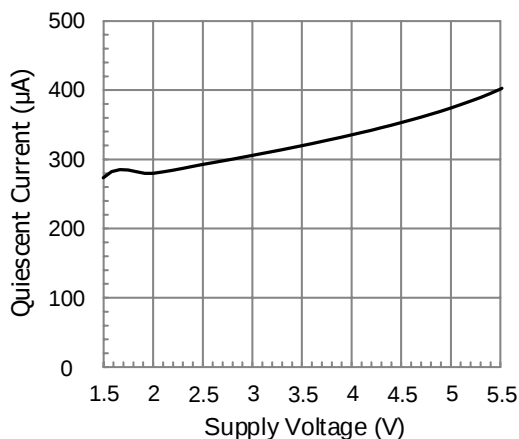


Figure 6. Quiescent Current vs. Supply Voltage

Typical Characteristics (continued)

$V_{CM} = V_S / 2$, and $R_L = 10k\Omega$ connected to $V_S/2$, at $T_A = +25^\circ\text{C}$, unless otherwise noted.

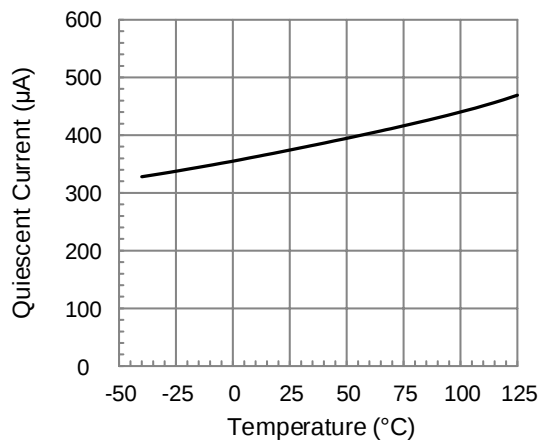


Figure 7. Quiescent Current vs. Temperature

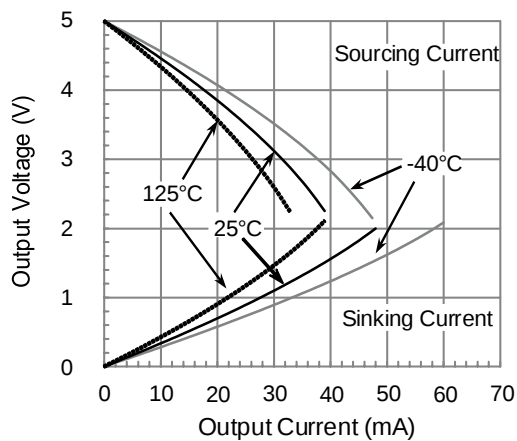


Figure 8. Output Voltage Swing vs. Output Current

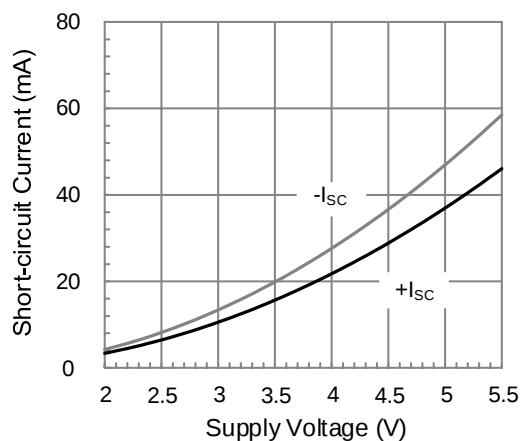


Figure 9. Short-circuit Current vs. Supply Voltage

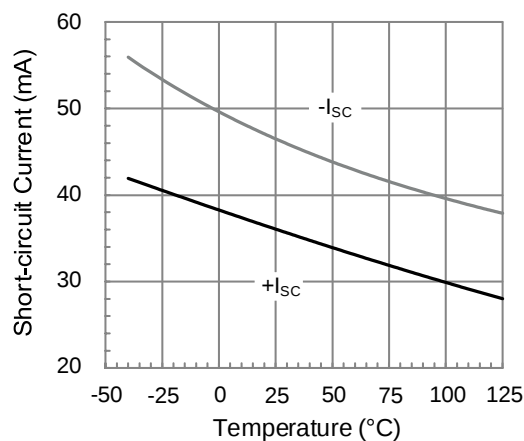


Figure 10. Short-circuit Current vs. Temperature

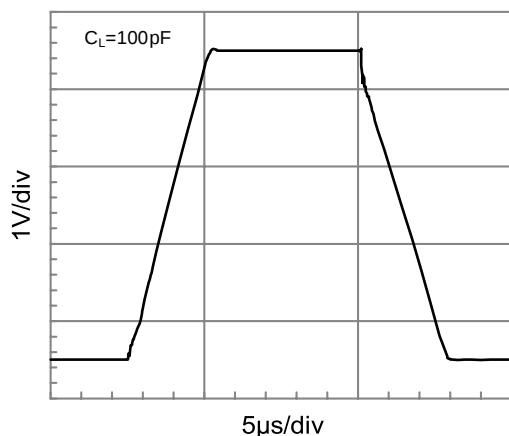


Figure 11. Large Signal Step Response

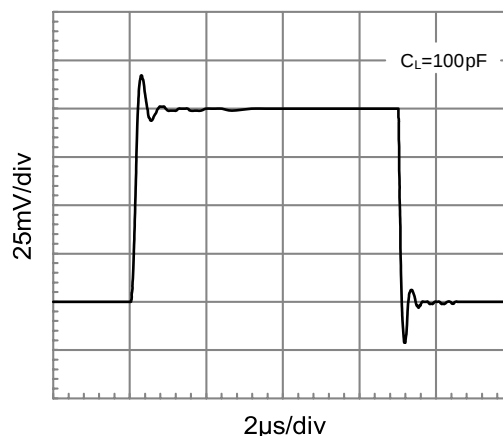


Figure 12. Small Signal Step Response

6 Functional Description

The GD30AP324H operational amplifier is unity-gain stable and free from unexpected output phase reversal. These devices use proprietary techniques to provide positive low offset voltage and low drift over temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifiers and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of $0.1\mu\text{V}/^{\circ}\text{C}$ or higher, depending on materials used.

6.1 Operating Voltage

The GD30AP324H family is fully specified and ensured for operation from 2.0V to 5.5V ($\pm 1.0\text{V}$ to $\pm 2.75\text{V}$). In addition, many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that vary significantly with operating voltages or temperature are illustrated in the [Typical Characteristics](#) graphs.

NOTE: Supply voltages (V_{S+} to V_{S-}) higher than +10 V can permanently damage the device.

6.2 Rail-to-Rail Input

The input common-mode voltage range of the GD30AP324H series extends 100mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically $V_{S+}-1.4\text{V}$ to the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately $V_{S+}-1.4\text{V}$. There is a small transition region, typically $V_{S+}-1.2\text{V}$ to $V_{S+}-1\text{V}$, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from $V_{S+}-1.4\text{V}$ to $V_{S+}-1.2\text{V}$ on the low end, up to $V_{S+}-1\text{V}$ to $V_{S+}-0.8\text{V}$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the GD30AP324H during normal operation is approximately 1pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

6.3 Input EMI Filter and Clamp Circuit

Figure 13 shows the input EMI filter and clamp circuit. The GD30AP324H op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 20mA as stated in the [Absolute Maximum Ratings](#).

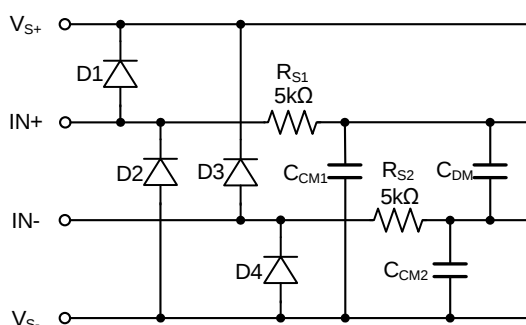


Figure 13. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the GD30AP324H family is composed of two 5kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the -3dB low-pass cutoff frequencies at 35MHz for common-mode signals, and at 22MHz for differential signals. Package Information

6.4 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the GD30AP324H delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 100kΩ, the output swings typically to within 5mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 2kΩ, the output swings typically to within 65mV of the positive supply rail and within 42mV of the negative supply rail.

6.5 Capacitive Load and Stability

The GD30AP324H family can safely drive capacitive loads of up to 500pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the GD30AP324H op-amps must drive a load exceeding 500pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO} , between

the amplifier output terminal and the load capacitance, as shown in Figure 14. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L .

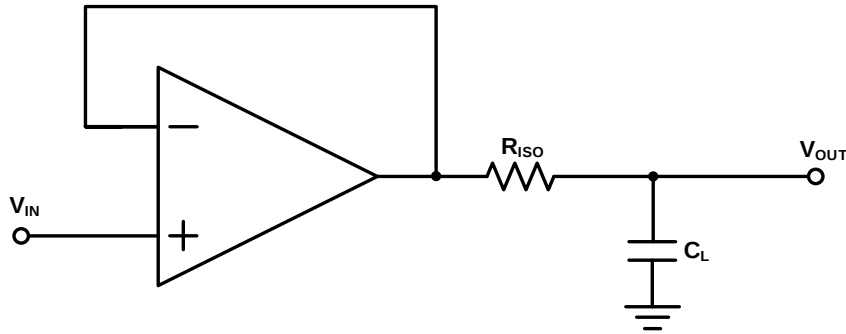


Figure 14. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 15. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

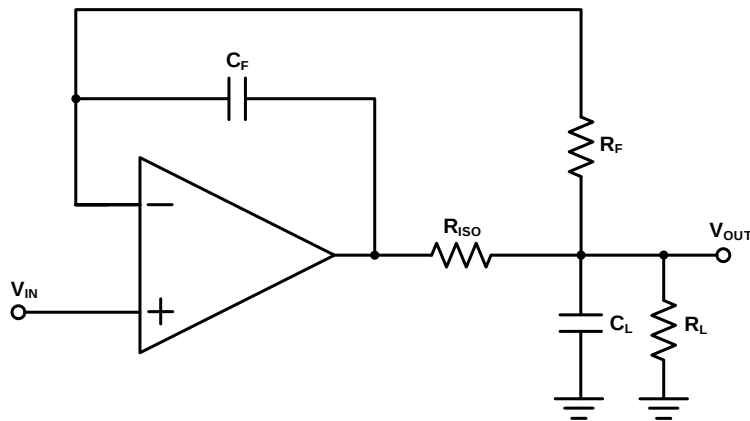


Figure 15. Indirectly Driving Heavy Capacitive Load with DC Accuracy

6.6 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the GD30AP324H family is approximately 2.5 μ s.

6.7 EMI Rejection Ratio

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The GD30AP324H op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$\text{EMIRR} = 20 \times \log \left(\frac{V_{\text{IN_PEAK}}}{\Delta V_{\text{OS}}} \right) \quad (1)$$

6.8 Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

6.9 Maximizing Performance Through Proper Layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the GD30AP324H op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 16 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

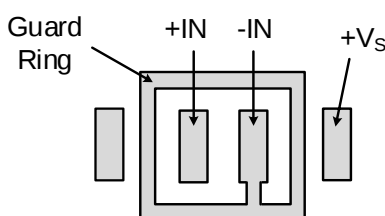


Figure 16. Use a Guard Ring around Sensitive Pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-

component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

7 Application Information

7.1 Typical Application Circuit

7.1.1 Differential Amplifier

The circuit shown in Figure 17 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$$V_{OUT} = (V_P - V_N) \times \frac{R_2}{R_1} + V_{REF} \quad (2)$$

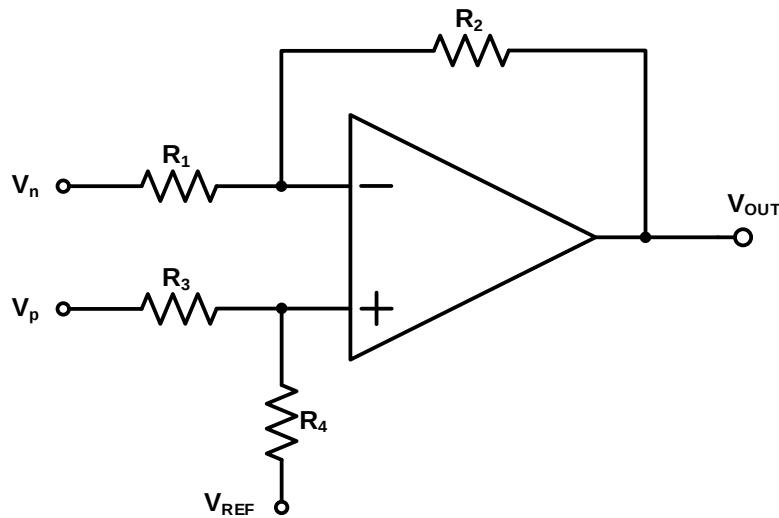


Figure 17. Differential Amplifier

7.1.2 Instrumentation Amplifier

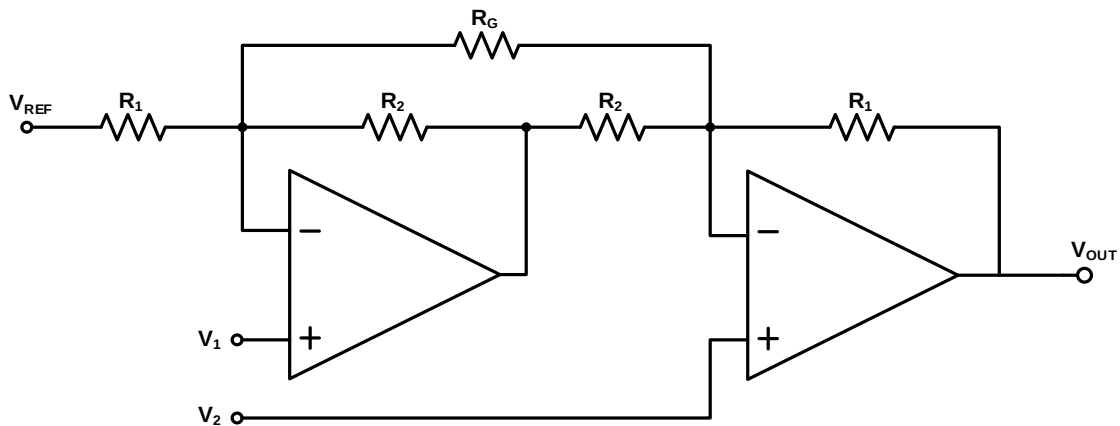


Figure 18. Instrumentation Amplifier

The GD30AP324H family is well suited for conditioning sensor signals in battery-powered applications. Figure 18 shows a two op-amp instrumentation amplifier, using the GD30AP324H op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

$$V_{OUT} = (V_2 - V_1) \times \left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G} \right) + V_{REF} \quad (3)$$

7.1.3 Buffered Chemical Sensors

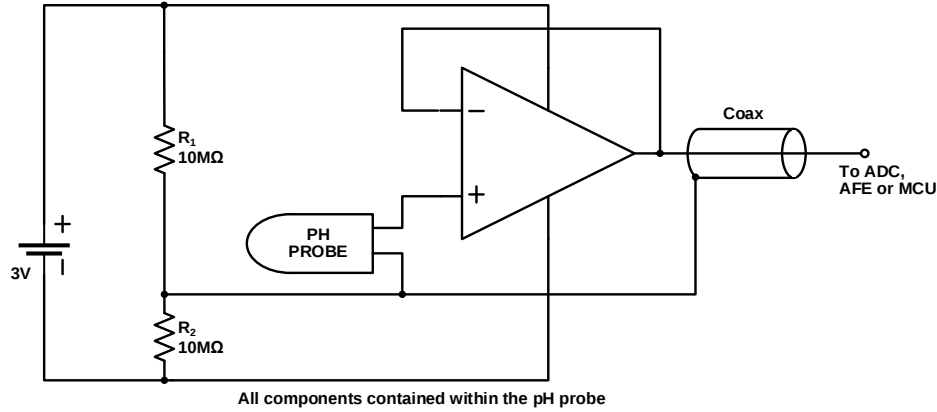


Figure 19. Buffered pH Probe

The GD30AP324H family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in [Figure 19](#) eliminates expensive low-leakage cables that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. A GD30AP324H op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

7.1.4 Motor Phase Current Sensing

The current sensing amplification shown in [Figure 20](#) has a slew rate of $2\pi fV_{PP}$ for the output of sine wave signal, and has a slew rate of $2fV_{PP}$ for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10KHz to 20KHz, and one cycle time is $100\mu s$ for a 10KHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the [Figure 20](#) shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t_{SR}) due to the op-amp's slew rate, and the measurement settling time (t_{SET}). For a 3-shunt solution in motor phase current sensing, if the smaller duty cycle of the PWM is defined at 45% (In fact, the phase with minimum PWM duty cycle, such as 5%, is not detected current directly, and it can be calculated from the other two phase currents), and the t_{SR} is required at 20% of a total time window for a phase current monitoring, in case of a 3.3V motor control system (3.3V MCU with 12-bit ADC), the op-amp's slew rate should be more than:

$$\frac{3.3V}{100\mu s \times 45\% \times 20\%} = 0.37V / \mu s \quad (4)$$

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.

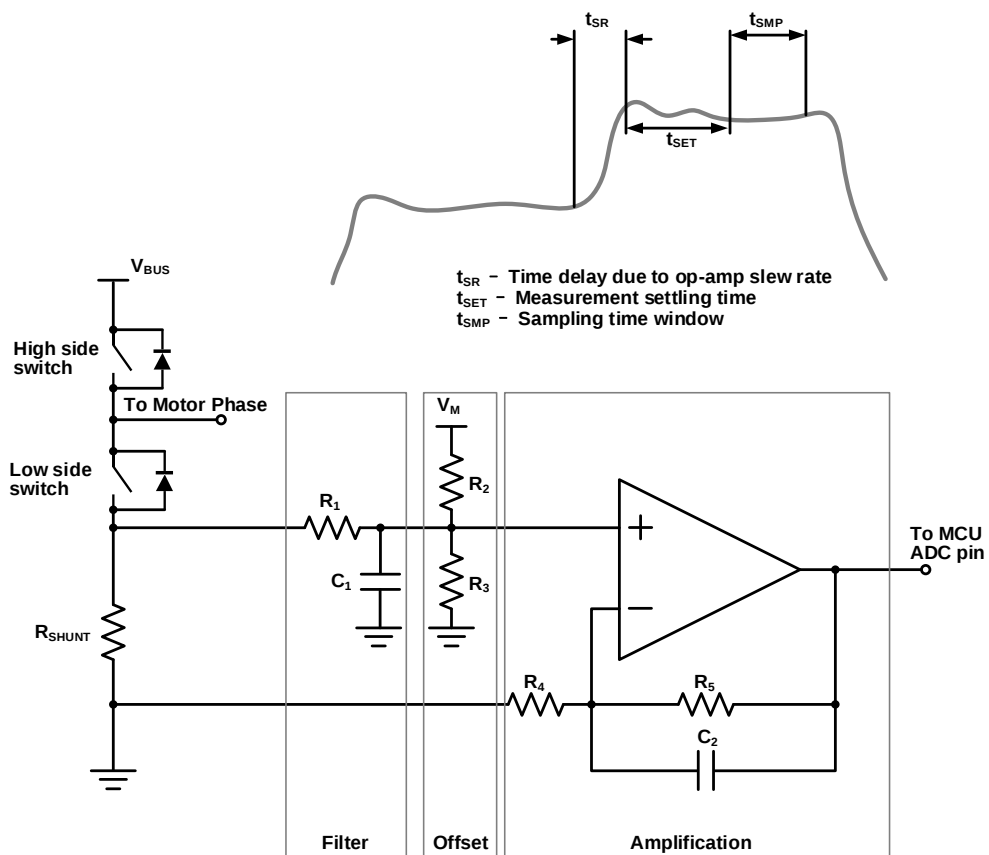
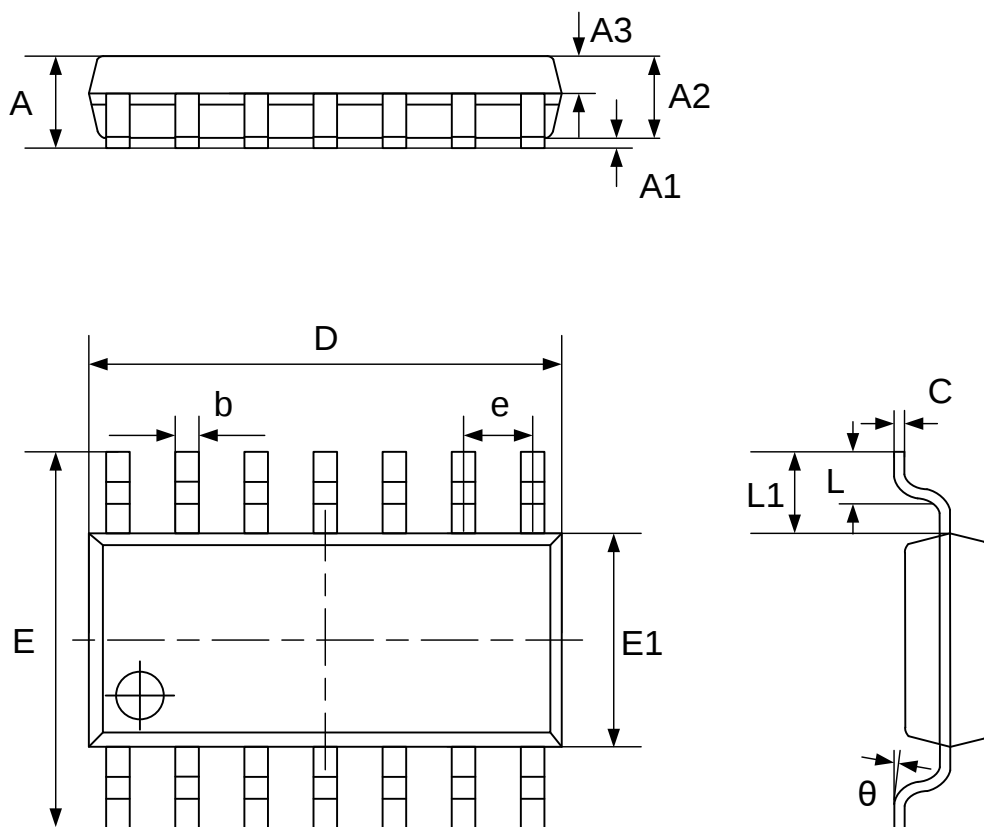


Figure 20. Current Shunt Monitor Circuit

8 Package Information

8.1 Outline Dimensions

SOIC-14L Package Outline



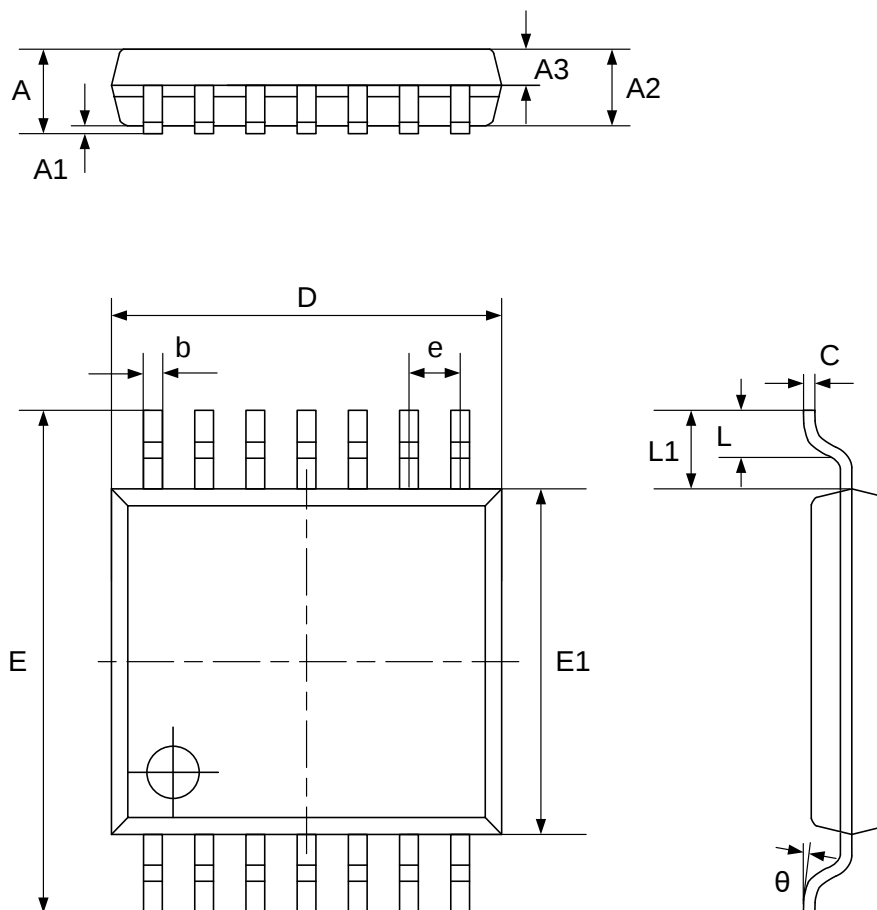
NOTES: (continued)

1. Refer to the [Table 1 SOIC-14L dimensions\(mm\)](#).

Table 1. SOIC-14L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	1.450		1.850
A1	0.100		0.300
A2	1.350		1.550
A3	0.550		0.750
b		0.406	
C		0.203	
D	8.630		8.830
E	5.840		6.240
E1	3.850		4.050
e		1.270	
L1	1.040 REF		
L	0.350		0.750
θ	2°		8°

TSSOP-14L Package Outline



NOTES: (continued)

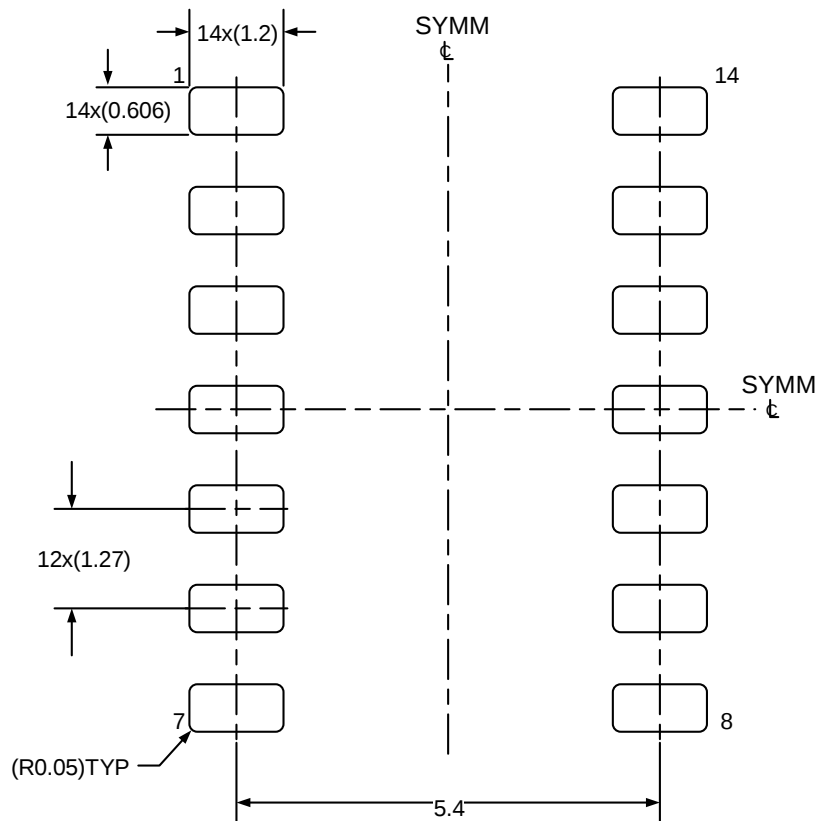
1. Refer to the [Table 2 TSSOP-14L dimensions\(mm\)](#).

Table 2. TSSOP-14L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A			1.200
A1	0.050		0.150
A2	0.900		1.050
A3	0.390		0.490
b	0.200		0.290
C	0.130		0.180
D	4.860		5.060
E	6.200		6.600
E1	4.300		4.500
e		0.650	
L1	1.000 REF		
L	0.450		0.750
θ	0°		8°

8.2 Recommended Land Pattern

SOIC-14L Land Pattern Example

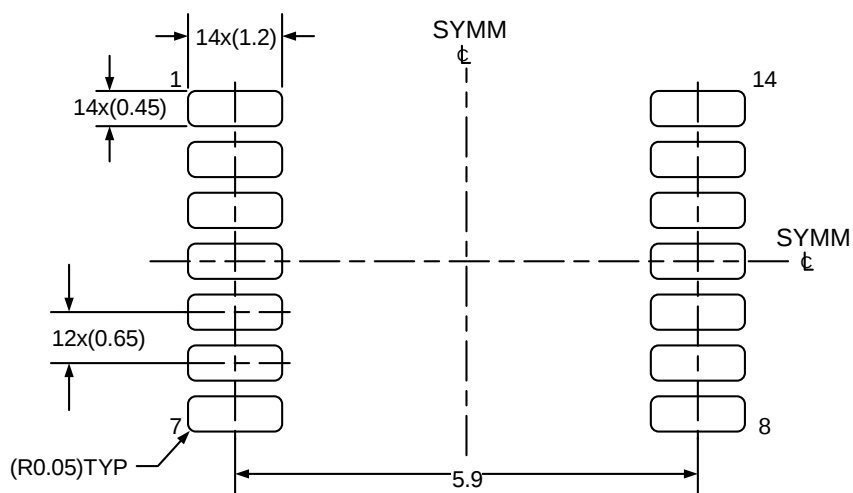


NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.

3. Drawing is 10X scale.

TSSOP-14L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30AP324HZLTR-I04	SOIC-14L	Green	Tape & Reel	2500	−40°C to +125°C
GD30AP324HZPTR-I04	TSSOP-14L	Green	Tape & Reel	3000	−40°C to +125°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2025

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