GD5F1GM9xExxG

3V/1.8V 1Gbit High-Speed Serial NAND Flash

Continuous Read & Cache Read

Contents

1 FEATURE

◆ 1Gb SLC NAND Flash

◆ Page Size

- Internal ECC On (ECC_EN=1, default):

Page Size：2048-Byte+64-Byte

- Internal ECC Off (ECC_EN=0):

Page Size：2048-Byte+128-Byte

◆ Standard, Dual, Quad SPI, DTR

- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- DTR (Double Transfer Rate) Read: SCLK, CS#, SIO0, SIO1, SIO2, SIO3

◆ High Speed Clock Frequency

- 3.3V:

166MHz for Standard/Dual/Quad SPI

133MHz for DTR Quad SPI

- 1.8V:

133MHz for Standard/Dual/Quad SPI

104MHz for DTR Quad SPI

◆ Software/Hardware Write Protection

- Write protect all/portion of memory via software
- Register protection with WP# Pin
- Power Lock Down Protection

◆ Single Power Supply Voltage

- Full voltage range for 1.8V: 1.7V ~ 2.0V
- Full voltage range for 3.3V: 2.7V ~ 3.6V

◆ Advanced security Features

- 20K-Byte OTP Region

◆ Program/Erase/Read Speed

- Page Program time: 320us typical
- Block Erase time: 3ms typical
- Page read time: 150us maximum

◆ Low Power Consumption

- 30mA maximum active current
- 50mA maximum active current (CR mode)
- 50uA maximum standby current

◆ Enhanced access performance

- 2KByte cache for fast random read

◆ Advanced Feature for NAND

- Factory good block0~block255
- Deep Power Down (1.8V only)
- Continuous Read
- Cache Read
- Bad Block Management
- Auto Load Next Page

◆ Reliability

- P/E cycles with ECC: 80K
- Data retention: 10 Years

◆ Internal ECC

- 8bits /528byte

Note: 1. ECC is on default, which can be disabled by user.

2. The P/E cycles with ECC will be 60K at 105℃ operation temperature.

2 GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra-cost effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI-NOR and standard parallel NAND Flash, with advanced features.

- Total pin count is 8, including VCC and GND
- Density is 1Gb
- Superior write performance and cost per bit over SPI-NOR
- Significant low cost than parallel NAND

This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pin out from one density to another. The command sets resemble common SPI-NOR command sets, modified to handle NAND specific functions and added new features. GigaDevice SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

- **User-selectable internal ECC**. ECC parity is generated internally during a page program operation. When a page is read to the cache register, the ECC parity is detected and corrects the errors when necessary. The 64-bytes spare area is available even when internal ECC enabled. The device outputs corrected data and returns an ECC error status.
- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data.
- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correct by internal ECC when ECC enabled. The user can also change the default power on read page by special command.
- **Continuous Read.** The device provides a high speed read mode that can read out sequential page by a single read command.
- **Bad Block Management.** The Product offers a convenient method to manage the bad blocks logical address. This function allows the user to replace the bad block with the good block that exist at the shipment and after extensive use to ensure that the logical block address is available and continuous.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

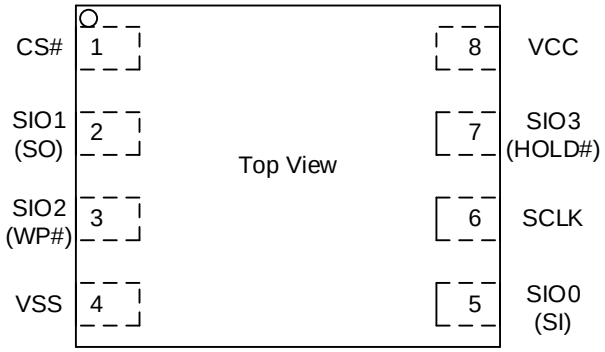
2.1 VALID PART NUMBERS

Please contact GigaDevice regional sales for the latest product selection and available form factors.

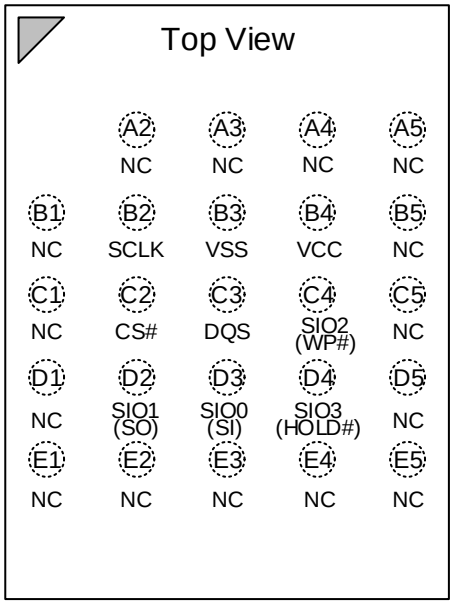
Product Number	Density	Voltage	Package Type	Temperature
GD5F1GM9REYIG	1Gbit	1.7V to 2.0V	WSON8 (8*6mm)	-40℃ to 85℃
GD5F1GM9REBIG			TFBGA24 (5*5 Ball Array)	-40℃ to 85℃
GD5F1GM9REWIG			WSON8 (6*5mm)	-40℃ to 85℃
GD5F1GM9UEYIG		2.7V to 3.6V	WSON8 (8*6mm)	-40℃ to 85℃
GD5F1GM9UEBIG			TFBGA24 (5*5 Ball Array)	-40℃ to 85℃
GD5F1GM9UEWIG			WSON8 (6*5mm)	-40℃ to 85℃

2.2 CONNECTION DIAGRAM

Figure 2-1 Connect Diagram



8 – LEAD WSON



24-BALL TFBGA (5x5 ball array)

2.3 PIN DESCRIPTION

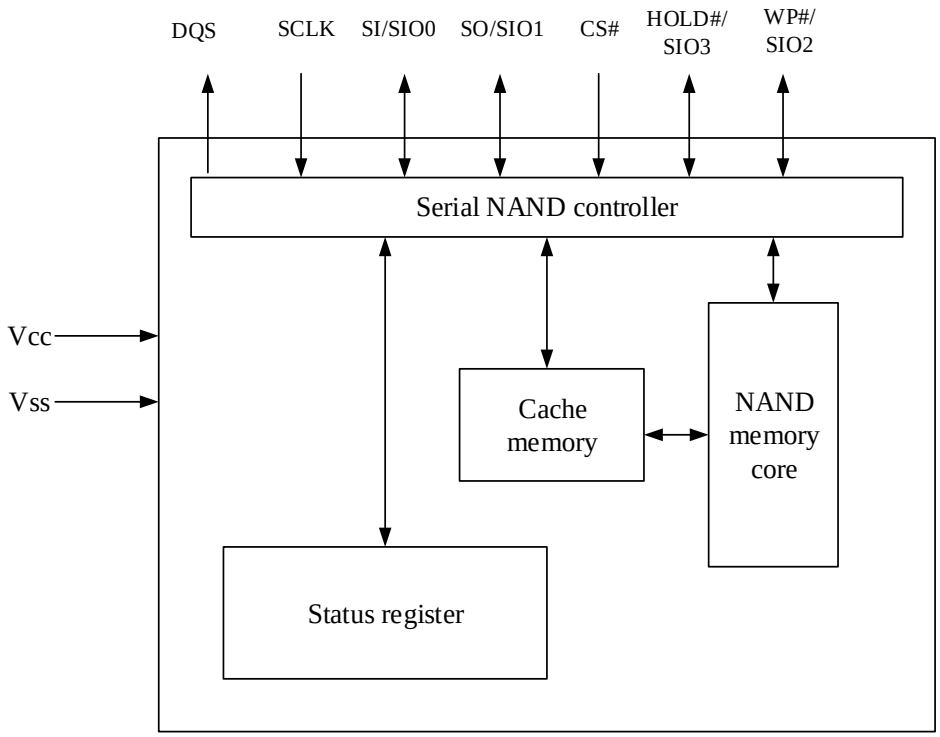
Pin Name	I/O	Description
CS#	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
VSS	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD# /SIO3	**I/O**	Hold Input/Serial Data Input Output 3
VCC	**Supply**	Power Supply
NC		Not Connect, Not internal connection; can be driven or floated.
DQS (only for BGA24)	**O**	Data Strobe Signal Output

Note：

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. If the DQS Function is not used, this pin must be floating.
3. If WP# and HOLD# are unused with QE=0, they are recommended be driven high by the host, or an external pull-up resistor should be placed on PCB in order to avoid allowing WP# and HOLD# driven low.
4. If SIO2 is unused with QE=1, it is recommended to be driven high or low by the host, or an external pull-up resistor should be placed on the PCB in order to avoid allowing SIO2 input to float.

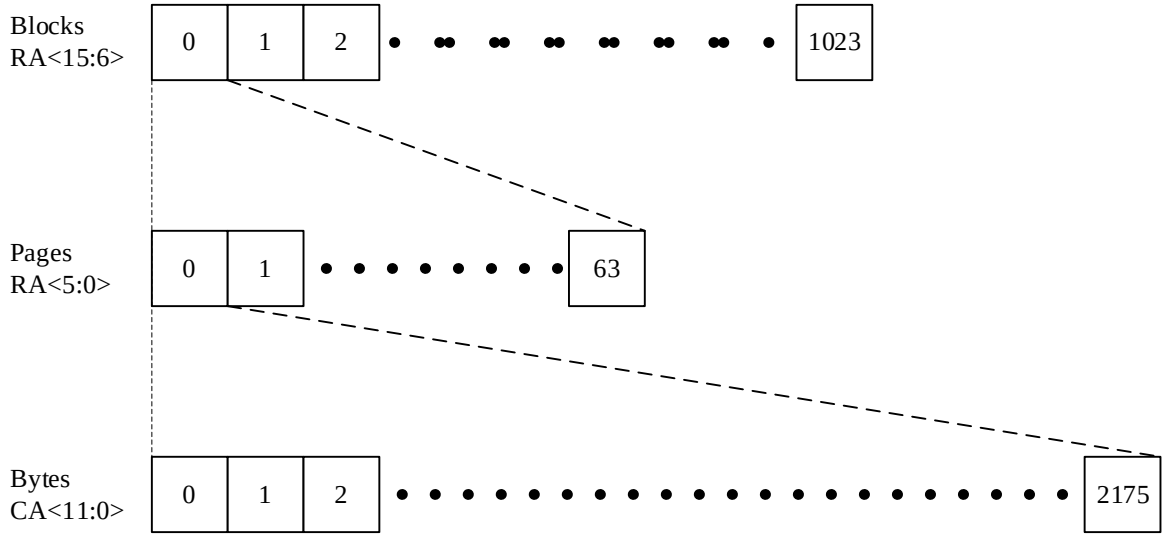
2.4 BLOCK DIAGRAM

Figure 2-2 Block Diagram



3 MEMORY MAPPING

For 1G



Note:

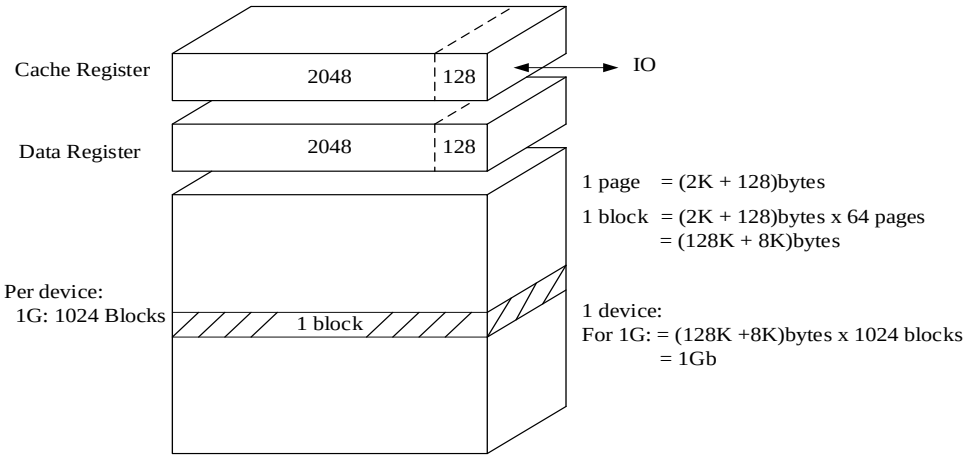
1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0>selects a page inside a block, and RA<15:6>selects a block.

4 ARRAY ORGANIZATION

Table 4-1. Array Organization

Each device has	Each block has	Each page has	
1Gb			
128M+8M	128K+8K	2K+128	bytes
1024 x 64	64	-	pages
1024	-	-	blocks

Figure 3-1. Array Organization



Note:

1.When Internal ECC is enabled，user can program the first 64 bytes of the entire 128 bytes spare area and the last 64 bytes of the whole spare area cannot be programed，user can read the entire 128 Byte spare area.

2.When Internal ECC is disabled，user can read and program the entire 128 bytes spare area.

5 DEVICE OPERATION

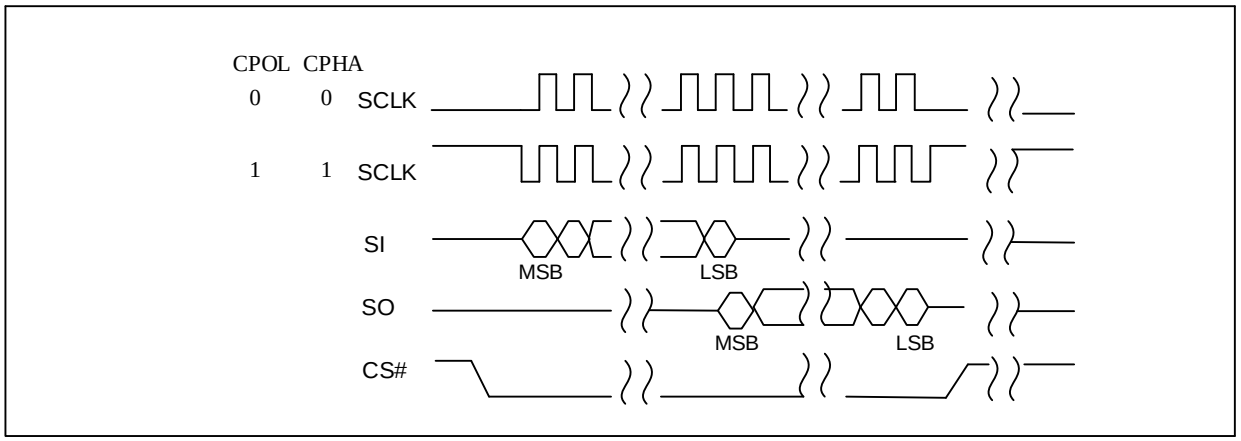
5.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. All timing diagrams shown in this data sheet are mode 0. See Figure5-1 for more details.

Figure 5-1. SPI Modes Sequence Diagram



Note: While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3). Do not toggle SCLK until CS# is driven LOW.

We recommend that the user pull CS# to high when user don't use SPI flash, otherwise the flash is always in the read state, which is damage for flash.

When CS# is high and SCLK at VCC or GND state, the device is in idle state.

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

DTR Quad SPI

The device supports DTR Quad SPI operation when using the “DTR Quad I/O Fast Read” command.

These commands allow data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. DTR Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be enable.

5.2 HOLD Mode

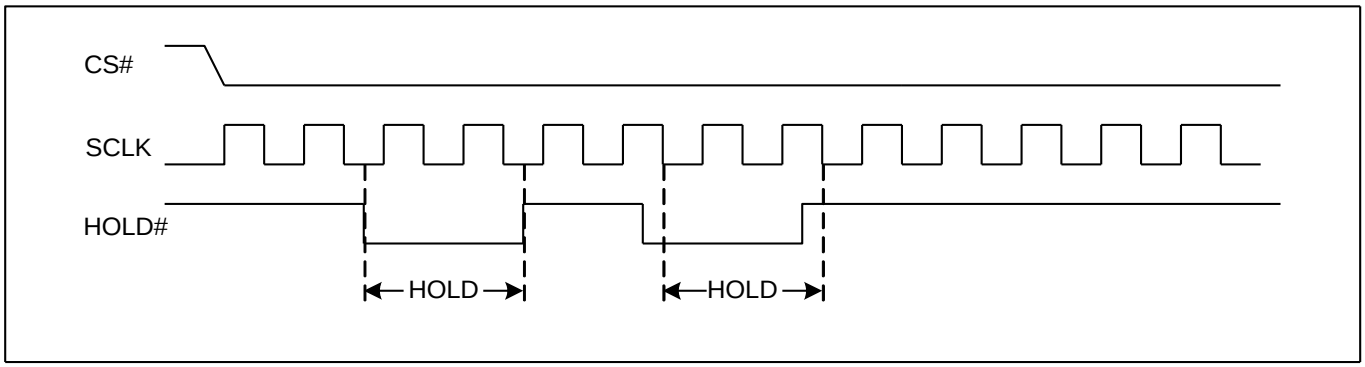
The HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of reading, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure 5-2. Hold Condition



5.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being over written. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

To enable the Write Protection, the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

5.4 Power Off Timing

Please do not turn off the power before Write/Erase operation is completed. Avoid using the device when the battery is low. Power shortage and/or power failure before Write/Erase operation is complete will cause loss of data and/or damage to data.

5.5 Data Strobe (DQS) signal

The DQS signal is an active output pin for the Data Strobe (DQS) signal during Read operations. The DQS signal is typically used in high speed applications to indicate when the output data is ready to be fetched by the controllers. To achieve such high frequency for specific DTR command, DQS pin is enabled on BGA24/SOP16 package of this device. DQS is only available in EDh/EEh command.

DQS signal is driven to ground once EDh/EEh command is accepted, and will start to toggle when the output data is ready on the I/O pins under DTR mode. The toggling frequency is the same as the CLK frequency. For DTR Read operations, the data should be latched on both rising edge and falling edge of the DQS signal.

If the DQS Function is not used, this pin must be floating.

5.6 Normal Read and Continuous Read Operation

The product provides two different modes for read operations, Normal Read Mode (NR=1) and Continuous Read Mode (NR=0). A Page Read to Cache command(13h) is needed to initiate the data transfer from a selected page in the memory array to the Cache Register before any read operation.

The Normal Read Mode (NR=1) is a general SPI NAND read mode. It requires a Column Address to start outputting the existing data in the Cache Register, and it outputs 2176 bytes in the page. Once it reaches the end of the Cache Register (Byte 2175), it will wrap around to the begin of the Cache Register (Byte 0). When another page needs to be read, the user need to resend a Page Read to Cache command to select the page.

The Continuous Read Mode (NR=0) doesn't require the starting Column Address. The device will always start output the data from the Byte0 of the Cache Register. And it outputs only 2048 bytes in the Main Area. Once it reaches the end of the page (Byte 2047), the data output will continue through the next page. In Continuous Read Mode, it can read out the entire memory array by a single read command. Therefore, the continuous read mode cannot avoid bad blocks. The data needs to be stored in consecutive good blocks to determine the correctness of the data read. The user can use the BBM function to replace the bad block with a good block. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read mode.

Table 5-1. Normal Read & Continuous Read Data Out Structure

NR	ECC_EN	Read Mode	Internal ECC Status	Data Output Structure
1	0	Normal Read	NA	2048+128
1	1	Normal Read (Default)	Page based	2048+128
0	0	Continuous Read	NA	2048
0	1	Continuous Read	Page based	2048

Table 5-2. Normal Read & Continuous Read Mode Function

NR	Read Mode	Cache Read Operation	Auto Load Next Page Feature (AL bit)
1(Default)	Normal Read	Available	Available
0	Continuous Read	NA	NA

Note:

In OTP Mode (OTP_EN enabled), the Read from Cache command (03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh) has the same format as normal read. The NR bit can't influence the OTP mode (OTP_EN enabled).

6 REGISTER AND FEATURE OPERATIONS

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to monitor the device status and alter the device behavior. Feature such as OTP can be enabled or disabled by setting specific feature bits. The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 6-1. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0h	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0h	OTP_PRT	OTP_EN	Reserved	ECC_EN	NR	Reserved	Reserved	QE
Status	C0h	Reserved	BBLS	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0h	Reserved	DS_S1	DS_S0	Reserved	DLP-EN	DC	Reserved	Reserved
Status	F0h	Reserved	Reserved	ECCSE1	ECCSE0	BPS	Reserved	Reserved	CBSY
Feature	60h	Reserved	Reserved	Reserved	Reserved	BPL	CRDC	AL	Reserved*
Feature	10h	BFT3	BFT2	BFT1	BFT0	Reserved	Reserved	Reserved	Reserved

Note: If BRWD is enabled and WP# is LOW, then the Protection Register cannot be changed.

If QE is enabled, the quad IO operations can be executed.

All the reserved bits must be held low when the feature is set.

These registers A0h/B0h/D0h/60h/10h are write/read type, and Registers C0h/F0h are read only.

Please refer to the below table of the Register Bit default value.

Please keep the 60h bit0 always to 0.

Table 6-2. A0h Features Register Bit Descriptions

Bit	Bit Name	Type	Default Value (After 66h-99h)	After Reset command (FFh)	Description
BRWD	Block register write disable	Volatile	0	No Change	This bit is used combined with WP#, If BRWD is set to 1 (enabled) and WP# is LOW, then the Protection Register (A0h) cannot be changed
BP2	Block Protection bits	Volatile	1	No Change	The Device offer the BP Protection by used combination. Please refer to the chapter Block Protection.
BP1		Volatile	1		
BP0		Volatile	1		
INV		Volatile	0		
CMP		Volatile	0		

Table 6-3. B0h Features Register Bit Descriptions

Bit	Bit Name	Type	Default Value (After 66h-99h)	After Reset command (FFh)	Description
OTP_PRT	OTP Region bits	OTP Lock	0 Before OTP Set	No Change	The Device offer the OTP Region by used combination. Please refer to chapter OTP Region
OTP_EN		Volatile	0		
ECC_EN	ECC Enable Latch	Volatile	1	No Change	The device offers data corruption protection by offering optional internal ECC. The internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on (ECC_EN=1).
NR	Normal Read Enable	Volatile	1	No Change	The device offers two different Read Mode. This bit can be written to change the mode between Normal Read and Continuous Read. 1: Normal Read Mode (Default) 0: Continues Read Mode
QE	The Quad Enable bit	Volatile	1	No Change	This bit indicates that whether the quad IO operations can be executed. 1: Quad enable 0: Quad not enable

Table 6-4. D0h Features Register Bit Descriptions

Bit	Bit Name	Type	Default Value (After 66h-99h)	After Reset command (FFh)	Description
DS_S1	Driven Strength register	Volatile	0	No Change	The device can change the IO driver strength setting by used combination. Please refer to the table Driver Register.
DS_S0		Volatile	0		
DLP-EN	Data Learning Pattern Enable	Volatile	0	No Change	This Feature bit can enable the Data Learning Pattern for Quad DTR Read commands (EDh, EEh) to determine the flash data output timing on 4 I/O pins. 1: DLP enable 0: DLP disable
DC	Dummy Configure	Volatile	0	No Change	This Feature bit can change the dummy clocks for higher frequency. and this bit is only available for BBh and EBh. Please refer to the dummy configure table.

Table 6-5. 60h Features Register Bit Descriptions

Bit	Bit Name	Type	Default Value (After 66h-99h))	After Reset command (FFh)	Description
BPL	Block Protection Lock register	Volatile	0	No Change	BPL is for Power Lock Down Protection. Once the BPL bit sets as 1, the rest of the protection bits BP [0,2], INV, CMP, BRWD can't be changed until next power cycle. By default BPL is 0 after power-on-reset and this bit default is Power Lock Down Protection disable.
CRDC	Continuous Read Dummy Configure	Volatile	0	No Change	This Feature bit can change the dummy clocks in continuous read mode for maintaining the same output timing as normal read mode. Please refer to the configure table.
AL	Auto Load Next Page	Volatile	0	No Change	The device offers the Function that auto load next page address to Cache Register during read operation. And shorten the tRD timing. Please refer to the chapter Auto Load Next Page. 1: Read Auto Load Next Page enable 0: Auto Load Next Page disable

Table 6-6. 10h Features Register Bit Descriptions

Bit	Bit Name	Type	Default Value (After 66h-99h)	After Reset command (FFh)	Description
bit flip threshold setting	BFT3	Volatile	1	No Change	This Feature bit can change the Internal ECC bit flip threshold. Only available in Continuous Read Mode A9h Command
	BFT2	Volatile	1	No Change	
	BFT1	Volatile	1	No Change	
	BFT0	Volatile	1	No Change	

Table 6-7. C0h/F0h Status Register Bit Descriptions

Bit	Bit Name	Type	Default Value (After 66h-99h)	After Reset command (FFh)	Description
ECCS1	ECC Status	Read only	Page 0 Status	0	This Status bit indicate the current page internal ECC status. They are then updated after the device completes a valid READ operation. Please refer to the chapter Internal ECC. ECCS and ECCSE are invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN to 0).After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.
ECCS0		Read only		0	
ECCSE1		Read only		0	
ECCSE0		Read only		0	
P_FAIL	Program Fail	Read only	0	0	This Status bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
E_FAIL	Erase Fail	Read only	0	0	This Status bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	Read only	0	0	This Status bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	Read only	0	0	This Status bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.

BPS	Block Protection Status	Read only	1	No Change	This Status bit indicates that whether the selected the block is protected. 1: Current block is protected 0: Current block is unprotected
CBSY bit	Cache Busy	Read only	0	0	This Status indicates the current status of the Cache Register. When the bit is 0, the Cache Register is in the ready state. It is useful in Cache Read Operation. 0: Cache Register Ready 1: Cache Register Busy
BBLS	Bad Block link Status	Read only	0	No Change	This bit indicates the current status of Bad Block Link Table. 0: bad block link is available and new bad block link can be added 1: All bad block links have been used

6.1 ECC Status Register and Driver Register

The NAND Flash device has an 8-bit status register that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0Fh) command, followed by the feature address C0h (see FEATURE OPERATION). The Output Driver Register can be set and read by issuing the SET FEATURE and GET FEATURE command followed by the feature address D0h (see FEATURE OPERATION).

Table 6-8. ECC Error Bits Descriptions

ECCS1	ECCS0	ECCSE1	ECCSE0	Description
0	0	x	X	No bit errors were detected during the previous read algorithm.
0	1	0	0	Bit errors(≤4) were detected and corrected.
0	1	0	1	Bit errors (=5) were detected and corrected.
0	1	1	0	Bit errors (=6) were detected and corrected.
0	1	1	1	Bit errors (=7) were detected and corrected.
1	1	x	X	Bit errors (=8) were detected and corrected.
1	0	x	X	Bit errors greater than ECC capability (8 bits) and not corrected.

Table 6-9. Driver Register Bits Descriptions by Design Trim

DS_S1	DS_S0	Driver Strength
0	0	100% (Default)
0	1	75%
1	0	50%
1	1	25%

6.2 Internal ECC

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on (ECC can also disable after power on, need contact with GD), so the default READ and PROGRAM commands operate with internal ECC in the “active” state when ECC enable.

To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1Fh) to set the feature bit ECC_EN:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC engine will verify and correct the data values according to the ECC code stored in spare area. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

The ECC protection formats as follow:

- All data in main area and spare areas data are protected.

Any data wrote to the ECC parity data area are ignored when ECC enabled.

Table 6-10. The Distribution of ECC Segment and Spare Area in a Page

Main Area(2KB)				Spare Area(128B)							
User data				User meta data				ECC Parity Data			
Main0	Main1	Main2	Main3	Spare0	Spare1	Spare2	Spare3	Spare0	Spare1	Spare2	Spare3
(512B)	(512B)	(512B)	(512B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)

Table 6-11. ECC Protection and Spare Area

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
80Fh	800h	Yes	Spare 0	User meta data 0(1)
81Fh	810h	Yes	Spare 1	User meta data 1
82Fh	820h	Yes	Spare 2	User meta data 2
83Fh	830h	Yes	Spare 3	User meta data 3
87Fh	840h	Yes	Spare Area	Internal ECC parity data

Note

1. 800h is reserved for initial bad block mark.
2. When ECC is on, the ECC for main/spare area (840H-87FH) is prohibited for user, but user can read the Address 840h~87Fh.
3. When ECC is off, the whole page area is open for user.

6.3 OTP Region

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 10 full pages are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0. To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, pages 02h–0Bh can be programmed in sequential order by PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands (when not yet protected), and read out by PAGE READ (13h) command and output data by READ FROM CACHE

When ECC is enabled, data written in the OTP area is ECC protected.

Table 6-12. OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region, read and program data
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10h) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data.

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

- Issue the SET FEATURES command (1Fh)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0Fh command.

- Issue the SET FEATURES command (1Fh)
- Set feature bit OTP_EN and OTP_PRT
- 06h (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10h) command

Note：

In OTP Mode (OTP_EN enabled), the Read from Cache command (03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh) has the same format as normal read mode. The NR bit can’t influence the OTP mode (OTP_EN enabled).

6.4 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1and BP2 are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0. When an ERASE command is issued to a locked block, the erase failure, status bit E_FAIL set to 1. When a PROGRAM command is issued to a locked block, program failure, status bit P_FAIL set to 1.

To enable the Write Protection (WP#), the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

Table 6-13. Block Lock Register Block Protect Bits (1Gb)

CMP	INV	BP2	BP1	BP0	Protect Row Address	Protect Rows
					1G	
x	x	0	0	0	None	None—all unlocked
0	0	0	0	1	FC00h～FFFFh	Upper 1/64 locked
0	0	0	1	0	F800h～FFFFh	Upper 1/32 locked
0	0	0	1	1	F000h～FFFFh	Upper 1/16 locked
0	0	1	0	0	E000h～FFFFh	Upper 1/8 locked
0	0	1	0	1	C000h～FFFFh	Upper 1/4 locked
0	0	1	1	0	8000h～FFFFh	Upper 1/2 locked
x	x	1	1	1	0000h～FFFFh	All locked (default)
0	1	0	0	1	0000h～03FFh	Lower 1/64 locked
0	1	0	1	0	0000h～07FFh	Lower 1/32 locked
0	1	0	1	1	0000h～0FFFh	Lower 1/16 locked
0	1	1	0	0	0000h～1FFFh	Lower 1/8 locked
0	1	1	0	1	0000h～3FFFh	Lower 1/4 locked
0	1	1	1	0	0000h～7FFFh	Lower 1/2 locked
1	0	0	0	1	0000h～FBFFh	Lower 63/64 locked
1	0	0	1	0	0000h～F7FFh	Lower31/32 locked
1	0	0	1	1	0000h～EFFFh	Lower 15/16 locked
1	0	1	0	0	0000h～DFFFh	Lower7/8 locked
1	0	1	0	1	0000h～BFFFh	Lower3/4 locked
1	0	1	1	0	0000h～003Fh	Block0
1	1	0	0	1	0400h～FFFFh	Upper 63/64 locked
1	1	0	1	0	0800h～FFFFh	Upper31/32 locked
1	1	0	1	1	1000h～FFFFh	Upper 15/16 locked
1	1	1	0	0	2000h～FFFFh	Upper7/8 locked
1	1	1	0	1	4000h～FFFFh	Upper3/4 locked
1	1	1	1	0	0000h～003Fh	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue SET FEATURES register write (1Fh)
- Issue the feature bit address (A0h) and the feature bits combination as the table

6.5 Hardware Write Protection

Hardware write protection prevents the block protection state from hardware modifications.

When BRWD is set and WP# is LOW, none of the writable protection feature bits [5:1] can be set.

Note: To enable the Write Protection (WP#), the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

6.6 Power Lock Down Protection

The Power lock down protection prevent the block protection state from software modifications. After it is enabled, this protection cannot be disabled by a software command. Also, BP [0,2], INV, CMP and BRWD bits are protected from further software change. Only another power cycle can disable the Power Lock Down Protection.

When the Hardware Protection is disabled during quad IO mode, Power Lock Down Protection can be used to prevent a block protection state change.

To enable the Power Lock Down Protection, perform the following command sequence:

- Issue the SET FEATURES command (with address 60h) to set the feature bit BPL to 1.

6.7 Auto Load Next Page Feature (AL bit)

The Device provide an acceleration read feature for sequential page read operation. When the Auto Load Next Page Feature bit is enabled (AL bit=1). the next page data from the memory array will be auto load into the date register during the previous page read time. After the data of previous page has been read in normal read, the user may issue a new Page Read to Cache command (13h) to read next page. Then the averaged tRD_ECC time will be shortened (Fast tRD_ECC). If the Page Read to Cache command (13h) selects the different page, there will be a normal tRD_ECC time. The Auto Load Next Page Feature is only available in Normal Read mode (NR=1) with Internal ECC enabled (ECC_EN=1).

6.8 Data Learning Pattern DLP

For Quad DTR Read commands (EDh/EEh), a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, the flash will output “00110100” Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output.

7 COMMANDS DESCRIPTION

Table 7-1. Commands Set (Except Read Command)

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte 7
Write Enable	06h						
Write Disable	04h						
Get Features	0Fh	A7-A0	D7-D0	Wrap (4)			
Set Feature	1Fh	A7-A0	D7-D0				
Read ID(1)	9Fh	Dummy	MID	DID1	DID2		
Read parameter page	13h	00h	00h	01h			
Read UID	13h	00h	00h	00h			
Program Load	02h	A15-A8	A7-A0	D7-D0	Next byte		
Program Load x4	32h	A15-A8	A7-A0	D7-D0	Next byte		
Program Execute	10h	A23-A16	A15-A8	A7-A0			
Program Load Random Data	84h	A15-A8	A7-A0	D7-D0	Next byte		
Program Load Random Data x4	C4h/34h	A15-A8	A7-A0	D7-D0	Next byte		
Block Erase(128K)	D8h	A23-A16	A15-A8	A7-A0			
Reset (2)	FFh						
Enable Power on Reset	66h						
Power on Reset (3)	99h						
Deep Power Down (1.8V Only)	B9h						
Release Deep Power Down (1.8V Only)	ABh						
Cache Read Sequential	31h						
Cache Read Random	30h	A23-A16	A15-A8	A7-A0			
Cache Read Random	13h	A23-A16	A15-A8	A7-A0	31h		
Cache Read End	3Fh						
Last ECC failure Page Address	A9h	Dummy	D7-D0	D7-D0			
ECC Status Read	7Ch	Dummy	D7-D0				
Write Auto power-on Page	A2h	A23-A16	A15-A8	A7-A0			
Bad Block Management (Swap Blocks)	A1h	LBA	LBA	PBA	PBA		
Read Bad Block Link Table	A5h	Dummy	LBA0	LBA0	PBA0	PBA0	LBA1
Page Read (to cache)	13h	A23-A16	A15-A8	A7-A0			

Note:

1. MID is Manufacture ID (C8h for GigaDevice), DID is Device ID.
2. Reset command:

• During busy, Reset will reset PAGE READ/PROGRAM/ERASE operation.

• During idle, Reset will reset status register bits P_FAIL/E_FAIL/WEL/OIP/ECCS/ECCSE.

3. Power on reset: Retrieve status register and data in cache to power on status.
4. The output would be updated by real-time, until CS# is driven high.
5. Read UID/parameter page/CASN page are same as page read to cache. And the Read from Cache command (03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh) has the same format as normal read mode.

Table 7-2. Read Command in Normal Read Mode (Default, NR Mode=1, CRDC=NA)

Read From Cache	03h	A15-A8	A7-A0	Dummy	D7-D0		
Fast Read From Cache	0Bh	A15-A8	A7-A0	Dummy	D7-D0		
Read From Cache with 4-Byte Address	0Ch	A15-A8	A7-A0	Dummy x3	D7-D0		
Read From Cache x2	3Bh	A15-A8	A7-A0	Dummy	(D7-D0) x2		
Read From Cache x2 with 4-Byte Address	3Ch	A15-A8	A7-A0	Dummy x3	(D7-D0) x2		
Read From Cache x4	6Bh	A15-A8	A7-A0	Dummy	(D7-D0) x4		
Read From Cache x4 with 4-Byte Address	6Ch	A15-A8	A7-A0	Dummy x3	(D7-D0) x4		
Read From Cache Dual IO	BBh	A15-A8	A7-A0	Dummy	(D7-D0) x2		
Read From Cache Dual IO with 4-Byte Address	BCh	A15-A8	A7-A0	Dummy x3	(D7-D0) x2		
Read From Cache Quad IO	EBh	A15-A8	A7-A0	Dummy x2	(D7-D0) x4		
Read From Cache Quad IO with 4-Byte Address	ECh	A15-A8	A7-A0	Dummy x5	(D7-D0) x4		
DTR Read From Cache Quad IO	EDh	A15-A8	A7-A0	Dummy x8	(D7-D0) x4		
DTR Read From Cache Quad IO with 4-Byte Address	EEh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy x8	(D7-D0) x4

Table 7-3. Read Command in Continuous Read Mode1 (NR Mode=0, CRDC=0)

Read From Cache	03h	Dummy x3	(D7-D0)				
Fast Read From Cache	0Bh	Dummy x4	(D7-D0)				
Read From Cache with 4-Byte Address	0Ch	Dummy x5	(D7-D0)				
Read From Cache x2	3Bh	Dummy x4	(D7-D0) x2				
Read From Cache x2 with 4-Byte Address	3Ch	Dummy x5	(D7-D0) x2				
Read From Cache x4	6Bh	Dummy x4	(D7-D0) x4				
Read From Cache x4 with 4-Byte Address	6Ch	Dummy x5	(D7-D0) x4				
Read From Cache Dual IO	BBh	Dummy x4	(D7-D0) x2				
Read From Cache Dual IO with 4-Byte Address	BCh	Dummy x5	(D7-D0) x2				
Read From Cache Quad IO	EBh	Dummy x6	(D7-D0) x4				
Read From Cache Quad IO with 4-Byte Address	ECh	Dummy x7	(D7-D0) x4				
DTR Read From Cache Quad IO	EDh	Dummy x11	(D7-D0) x4				
DTR Read From Cache Quad IO with 4-Byte Address	EEh	Dummy x12	(D7-D0) x4				

Table 7-4. Read Command in Continuous Read Mode2 (NR Mode=0, CRDC=1)

Read From Cache	03h	Dummy x3	(D7-D0)				
Fast Read From Cache	0Bh	Dummy x3	(D7-D0)				
Read From Cache with 4-Byte Address	0Ch	Dummy x5	(D7-D0)				
Read From Cache x2	3Bh	Dummy x3	(D7-D0) x2				
Read From Cache x2 with 4-Byte Address	3Ch	Dummy x5	(D7-D0) x2				
Read From Cache x4	6Bh	Dummy x3	(D7-D0) x4				
Read From Cache x4 with 4-Byte Address	6Ch	Dummy x5	(D7-D0) x4				
Read From Cache Dual IO	BBh	Dummy x3	(D7-D0) x2				
Read From Cache Dual IO with 4-Byte Address	BCh	Dummy x5	(D7-D0) x2				
Read From Cache Quad IO	EBh	Dummy x4	(D7-D0) x4				
Read From Cache Quad IO with 4-Byte Address	ECh	Dummy x7	(D7-D0) x4				
DTR Read From Cache Quad IO	EDh	Dummy x10	(D7-D0) x4				
DTR Read From Cache Quad IO with 4-Byte Address	EEh	Dummy x12	(D7-D0) x4				

Table 7-5. Read From Cache Command in Different Read Mode

		Normal Read Default				**Continuous Read (CRDC=0)**		**Continuous Read (CRDC=1)**	
Command	DC bit	Address	Dummy Clocks	Total	Frequency	Total	Frequency	Total	Frequency
03h	NA	A15~A0	8 Dummy	24 Clocks	166MHz (3V) 133MHz (1.8V)	24 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	24 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
0Bh	NA	A15~A0	8 Dummy	24 Clocks	166MHz (3V) 133MHz (1.8V)	32 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	24 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
0Ch	NA	A15~A0	24 Dummy	40 Clocks	166MHz (3V) 133MHz (1.8V)	40 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	40 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
3Bh	NA	A15~A0	8 Dummy	24 Clocks	166MHz (3V) 133MHz (1.8V)	32 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	24 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
3Ch	NA	A15~A0	24 Dummy	40 Clocks	166MHz (3V) 133MHz (1.8V)	40 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	40 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
6Bh	NA	A15~A0	8 Dummy	24 Clocks	166MHz (3V) 133MHz (1.8V)	32 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	24 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
6Ch	NA	A15~A0	24 Dummy	40 Clocks	166MHz (3V) 133MHz (1.8V)	40 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	40 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
BCh	NA	A15~A0	12 Dummy	20 Clocks	166MHz (3V) 133MHz (1.8V)	20 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	20 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
ECh	NA	A15~A0	10 Dummy	14 Clocks	166MHz (3V) 133MHz (1.8V)	14 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	14 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
EDh	NA	A15~A0	8 Dummy	10 Clocks	133MHz (3V) 104MHz (1.8V)	11 Dummy Clocks	83MHz (3V) 66MHz (1.8V)	10 Dummy Clocks	83MHz (3V) 66MHz (1.8V)
EEh	NA	A31~A0	8 Dummy	12 Clocks	133MHz (3V) 104MHz (1.8V)	12 Dummy Clocks	83MHz (3V) 66MHz (1.8V)	12 Dummy Clocks	83MHz (3V) 66MHz (1.8V)
BBh	DC=0	A15~A0	4 Dummy	12 Clocks	133MHz (3V) 104MHz (1.8V)	16 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	12 Dummy Clocks	133MHz (3V) 104MHz (1.8V)
	DC=1	A15~A0	8 Dummy	16 Clocks	166MHz (3V) 133MHz (1.8V)			16 Dummy Clocks	166MHz (3V) 133MHz (1.8V)
EBh	DC=0	A15~A0	4 Dummy	8 Clocks	133MHz (3V) 104MHz (1.8V)	12 Dummy Clocks	166MHz (3V) 133MHz (1.8V)	8 Dummy Clocks	133MHz (3V) 104MHz (1.8V)
	DC=1	A15~A0	8 Dummy	12 Clocks	166MHz (3V) 133MHz (1.8V)			12 Dummy Clocks	166MHz (3V) 133MHz (1.8V)

8 WRITE OPERATIONS

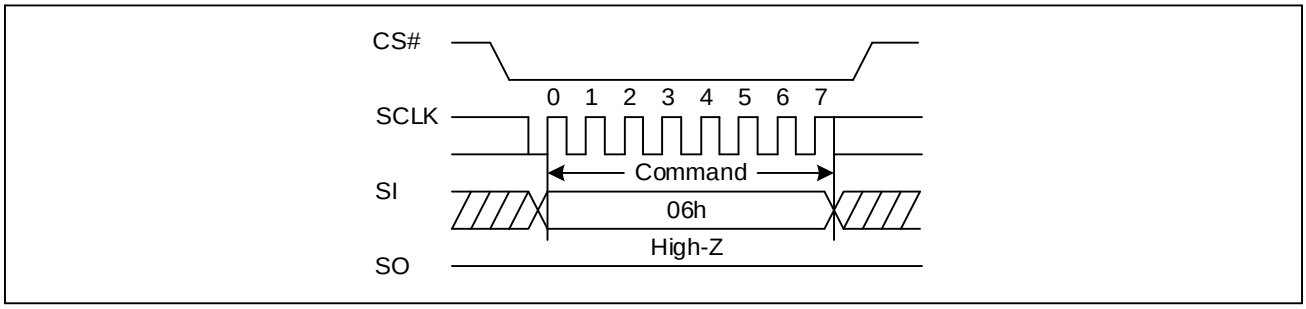
8.1 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Figure 8-1. Write Enable Sequence Diagram

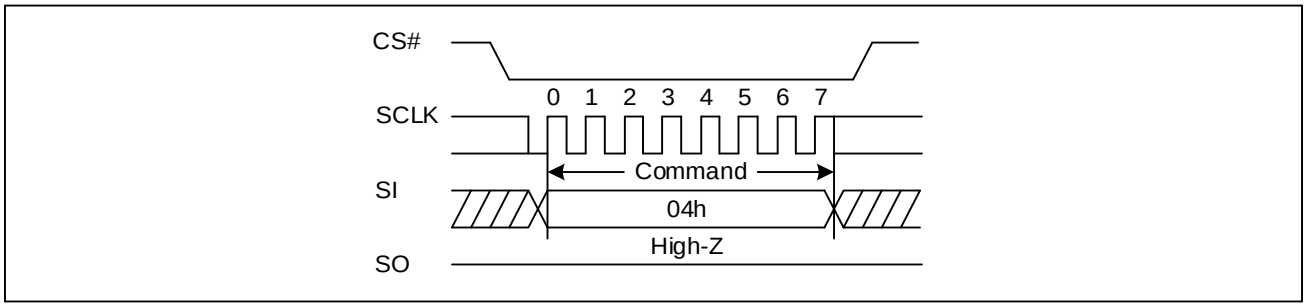


8.2 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Figure 8-2. Write Disable Sequence Diagram



9 FEATURE OPERATIONS

9.1 Get Features (0Fh) and Set Features (1Fh)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Please refer to the chapter Register and Feature Operation.

Figure 9-1. Get Features Sequence Diagram

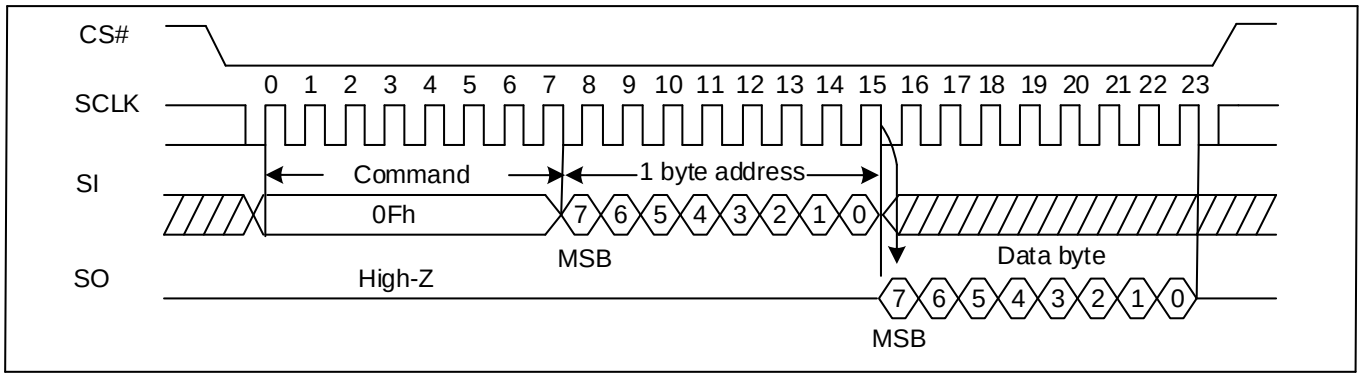
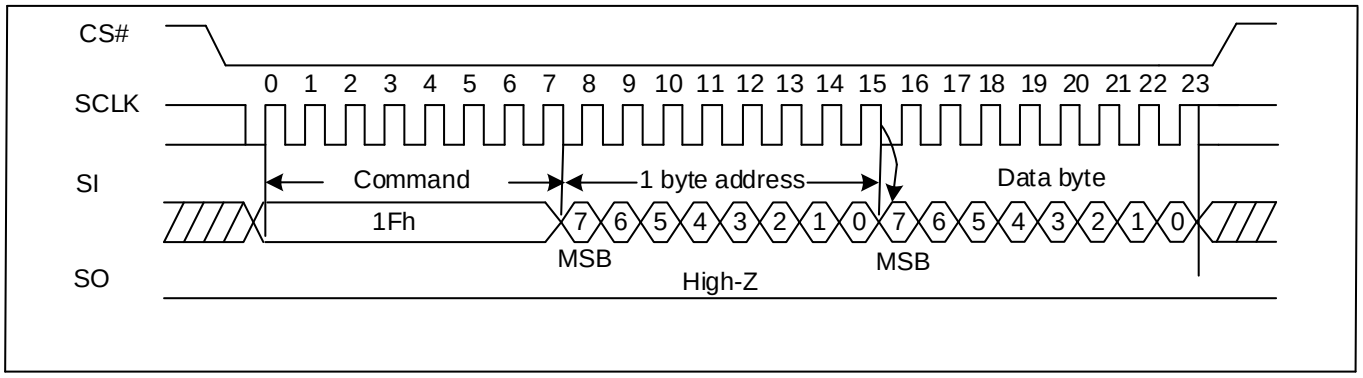


Figure 9-2. Set Features Sequence Diagram



10 READ OPERATIONS

10.1 Page Read

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURES command to read the status)
- 03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh(Read from cache command)

The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD w/o ECC time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status. Followed the page read operation, the Read from Cache command(03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh) must be issued in order to read out the data from cache.

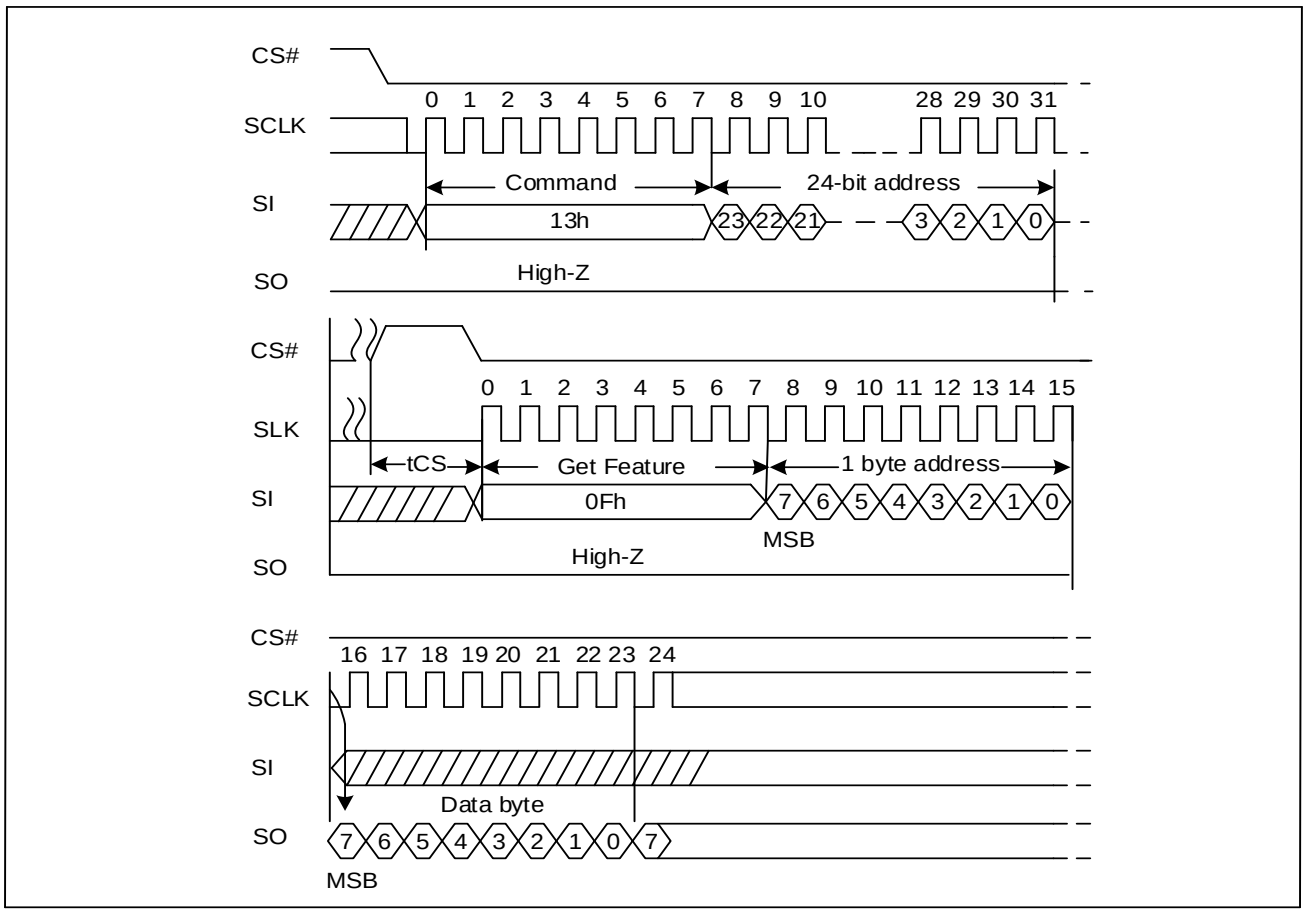
Note: (1) The command 6Bh/6Ch/EBh/ECh/EDh/EEh (Quad IO Read command) is only available with the QE enable.

(2) When user read to the end of 64-Byte spare area, it won't wrap around from the beginning boundary and an additional 64Byte ECC code will be read. (Internal ECC enabled)

10.2 Page Read to Cache (13h)

The command page read to cache is read the data from flash array to cache register.

Figure 10-1 Page Read to cache Sequence Diagram



10.3 Read From Cache (03h)

The command sequence is shown below.

Figure 10-2.a Normal Read(Default, NR=1)

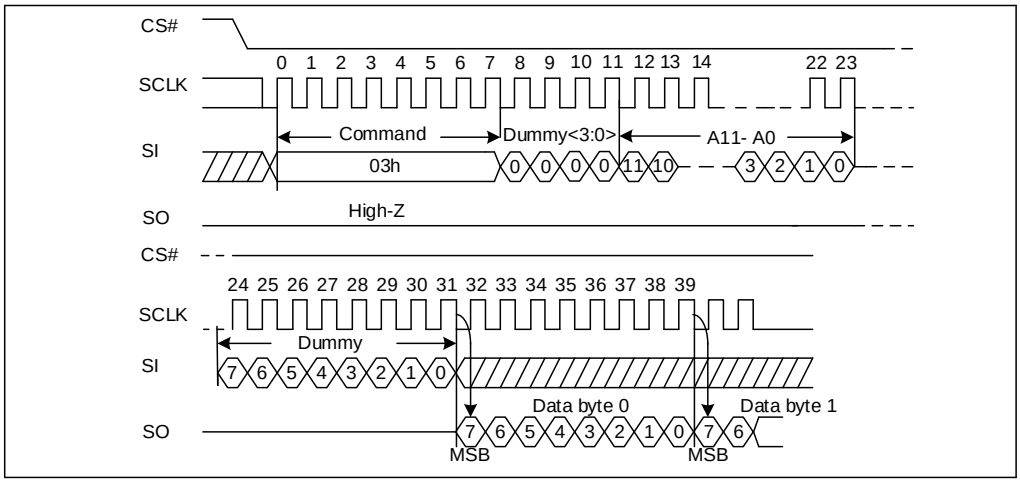


Figure 10-2.b Continuous Read Mode1 (NR=0, CRDC=0)

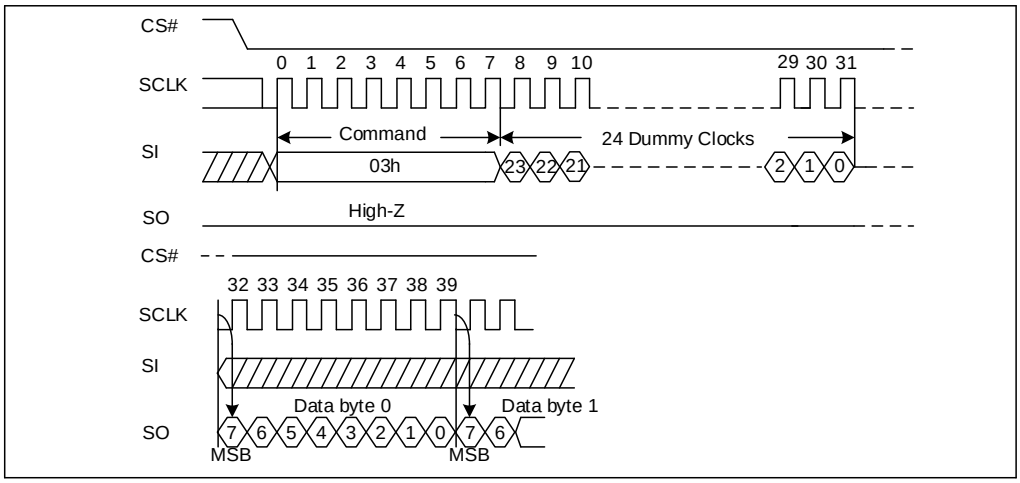
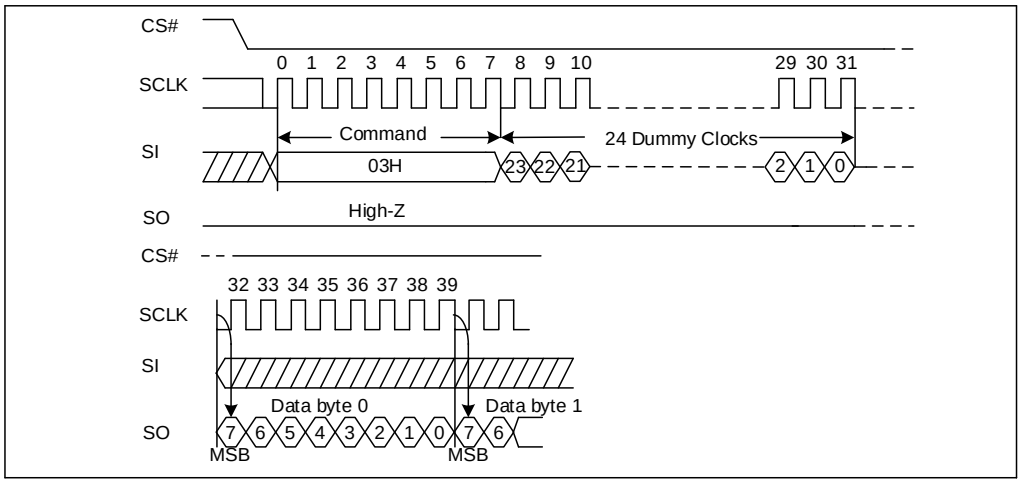


Figure 10-2.c Continuous Read Mode2 (NR=0, CRDC=1)



10.4 Fast Read From Cache (0Bh)

The command sequence is shown below.

Figure 10-3.a Normal Read (Default, NR=1)

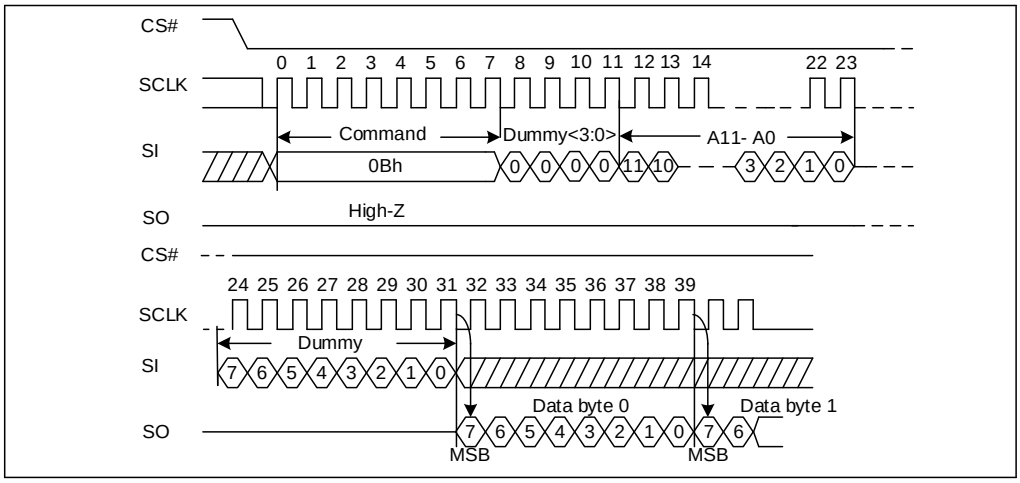


Figure 10-3.b Continuous Read Mode1 (NR=0, CRDC=0)

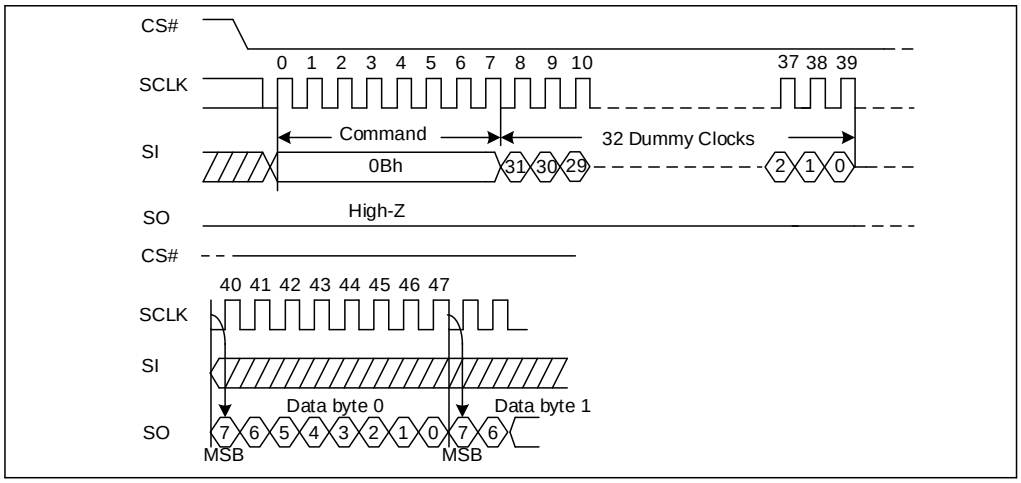
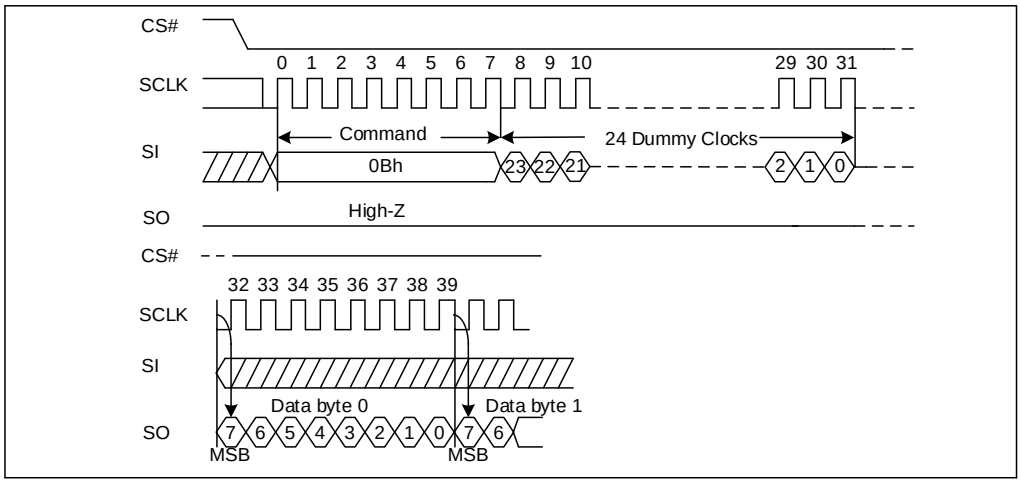


Figure 10-3.c Continuous Read Mode2 (NR=0, CRDC=1)



10.5 Read From Cache with 4-Byte Address (0Ch)

Figure 10-4.a Normal Read (Default, NR=1)

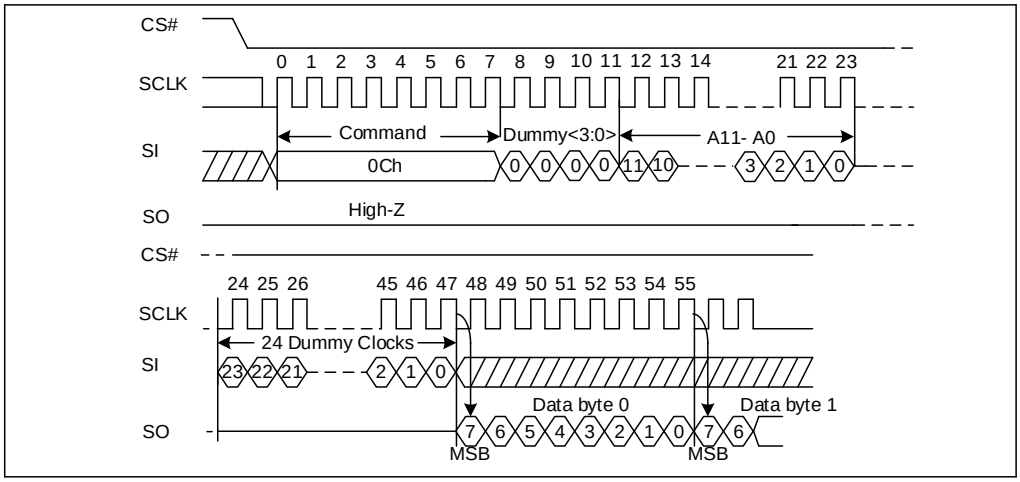


Figure 10-4.b Continuous Read Mode1 (NR=0, CRDC=0)

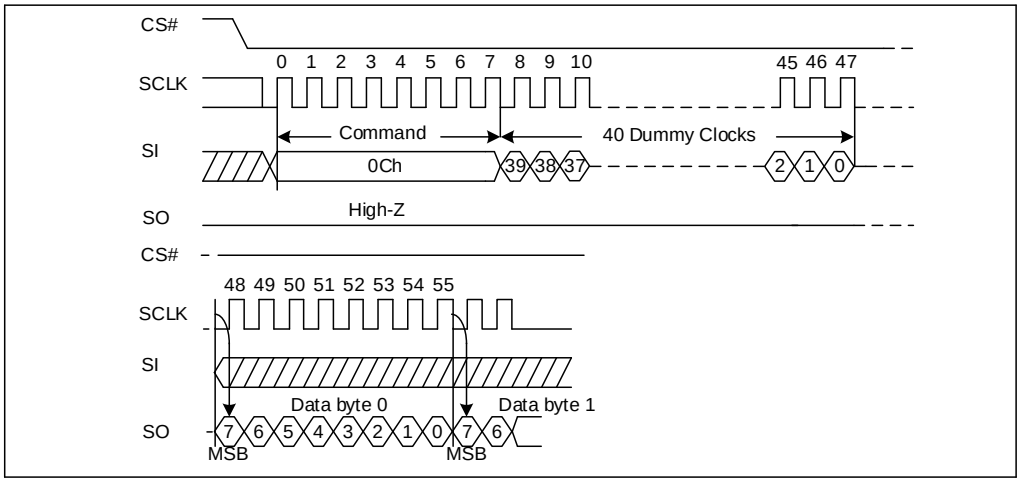
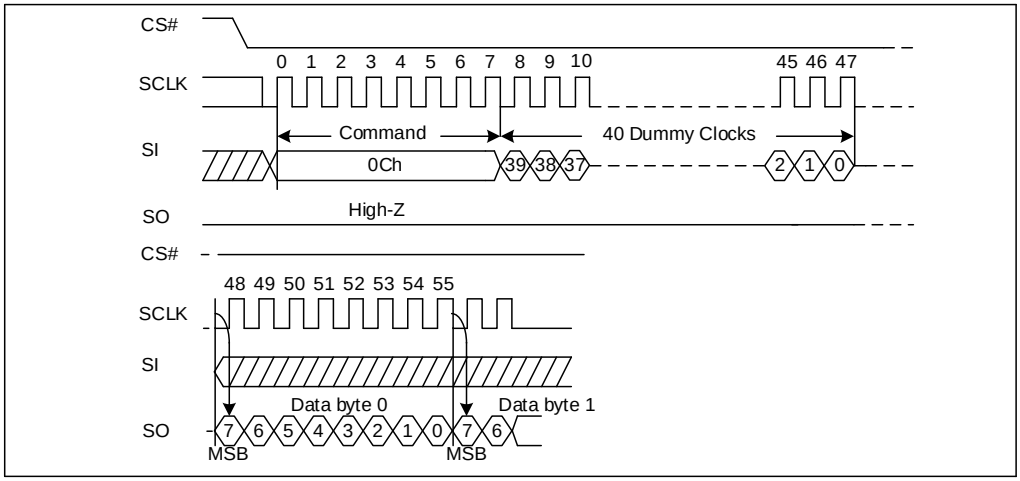


Figure 10-4.c Continuous Read Mode2 (NR=0, CRDC=1)



10.6 Read From Cache x2 (3Bh)

The command sequence is shown below.

Figure 10-5.a Normal Read (Default, NR=1)

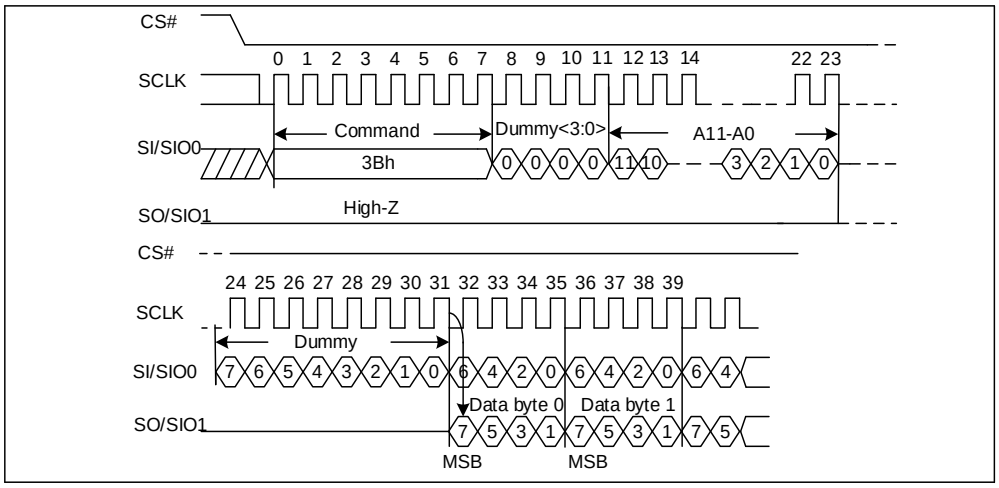


Figure 10-5.b Continuous Read Mode1 (NR=0, CRDC=0)

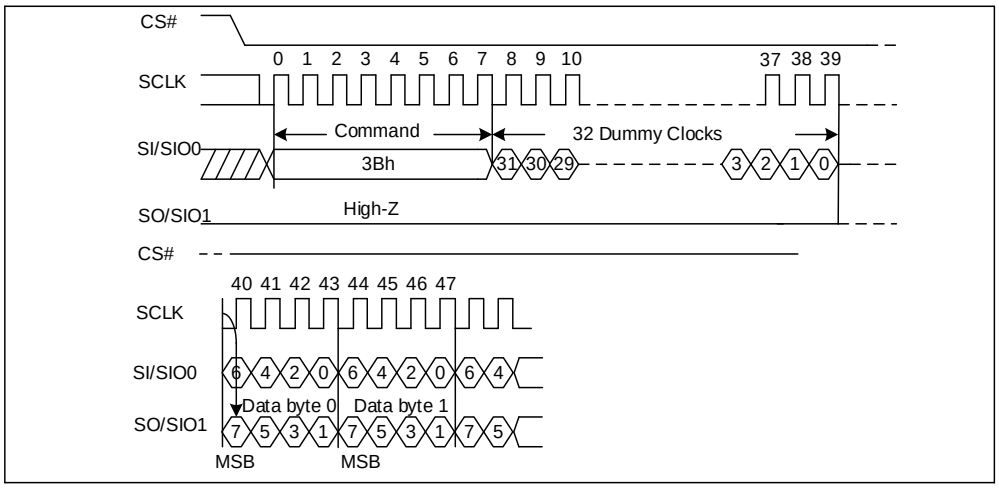
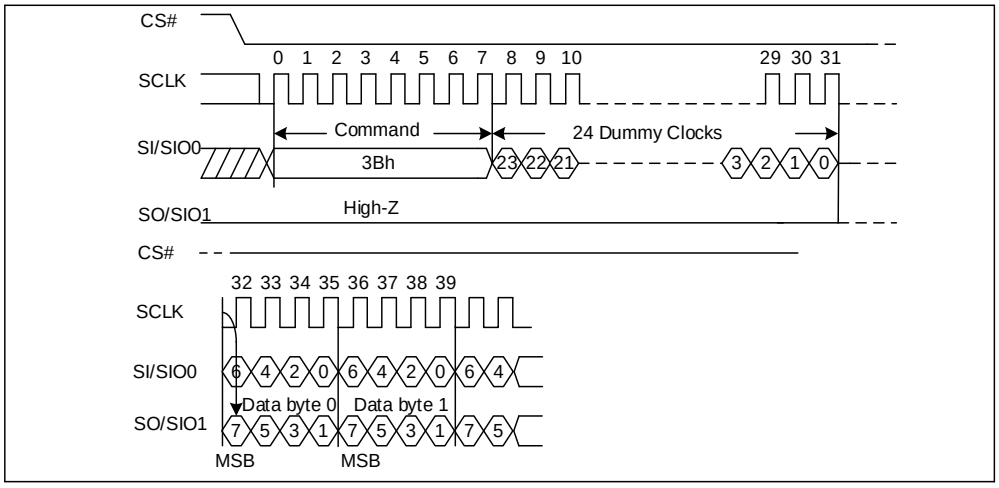


Figure 10-5.c Continuous Read Mode2 (NR=0, CRDC=1)



10.7 Read From Cache x2 with 4-Byte Address (3Ch)

Figure 10-6.a Normal Read (Default, NR=1)

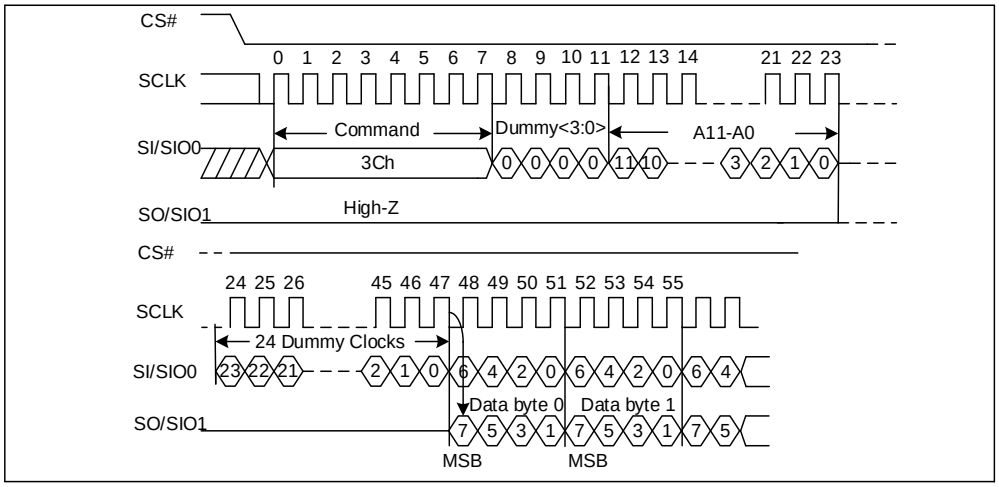


Figure 10-6.b Continuous Read Mode1 (NR=0, CRDC=0)

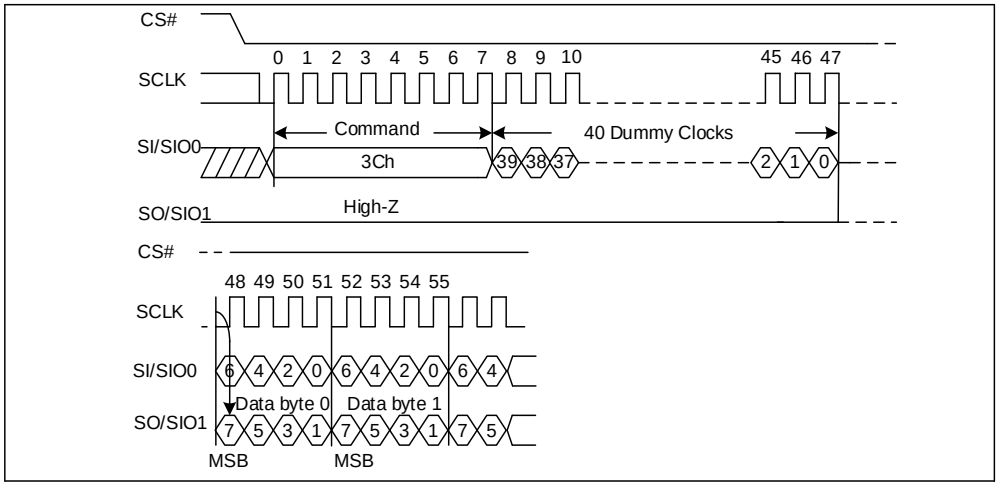
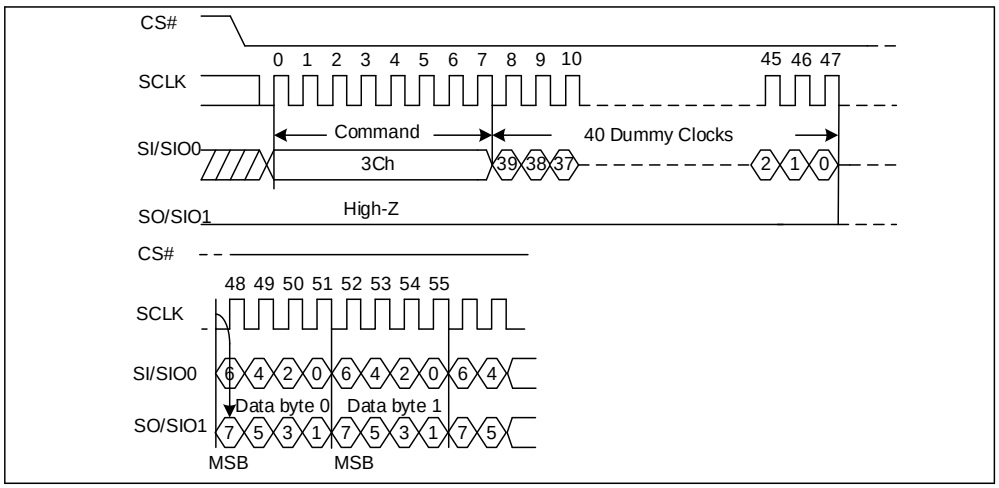


Figure 10-6.c Continuous Read Mode2 (NR=0, CRDC=1)



10.8 Read From Cache x4 (6Bh)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command. The command sequence is shown below.

Figure 10-7.a Normal Read (Default, NR=1)

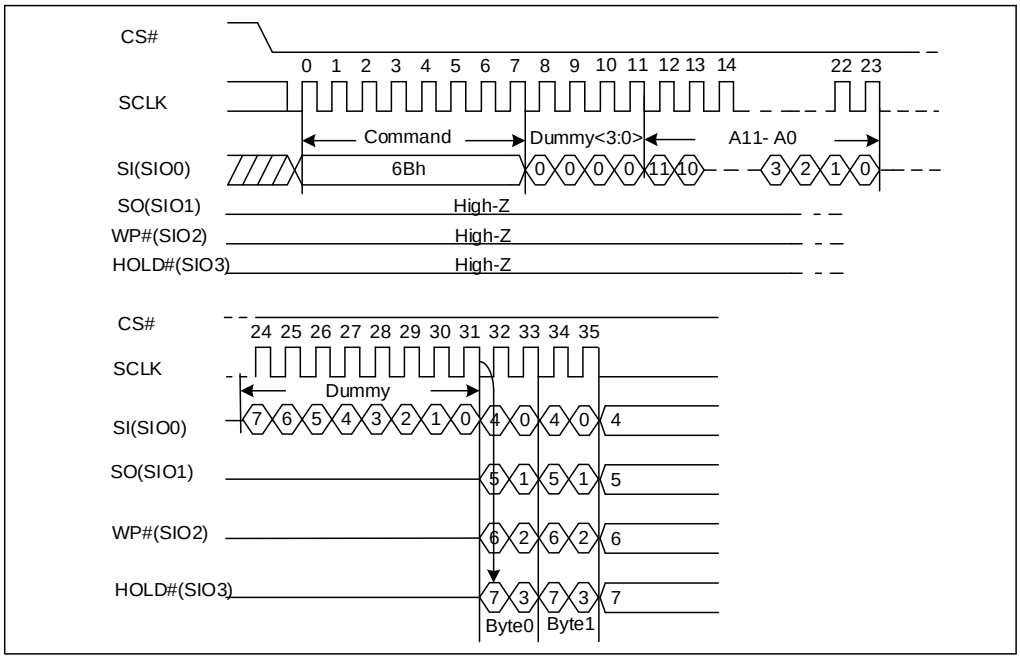


Figure 10-7.b Continuous Read Mode1 (NR=0, CRDC=0)

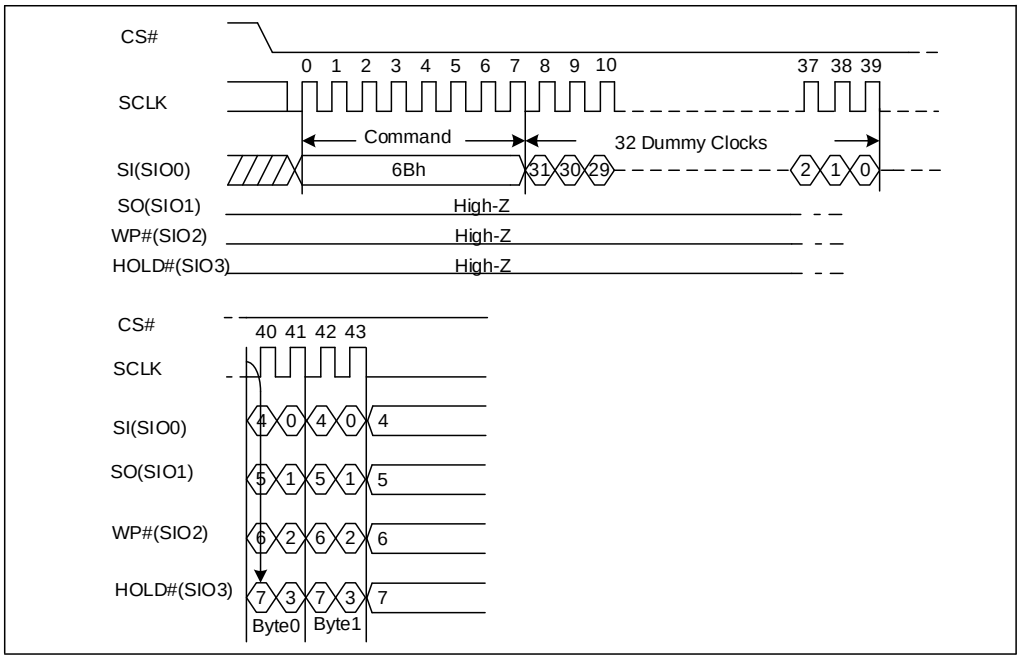
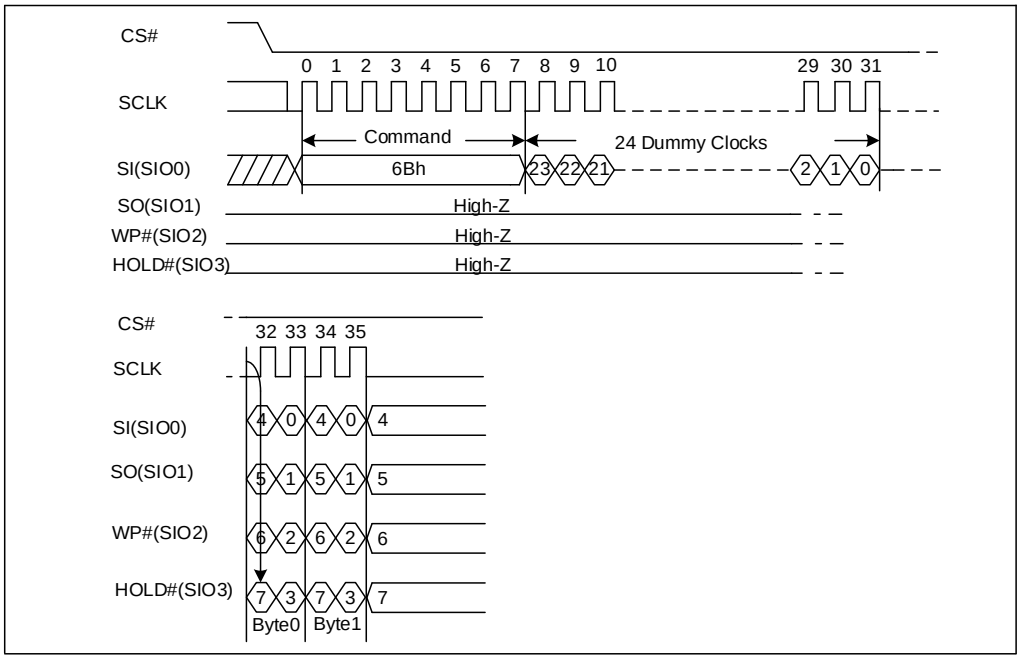


Figure 10-7.c Continuous Read Mode2 (NR=0, CRDC=1)



10.9 Read From Cache x4 with 4-Byte Address (6Ch)

Figure 10-8.a Normal Read (Default, NR=1)

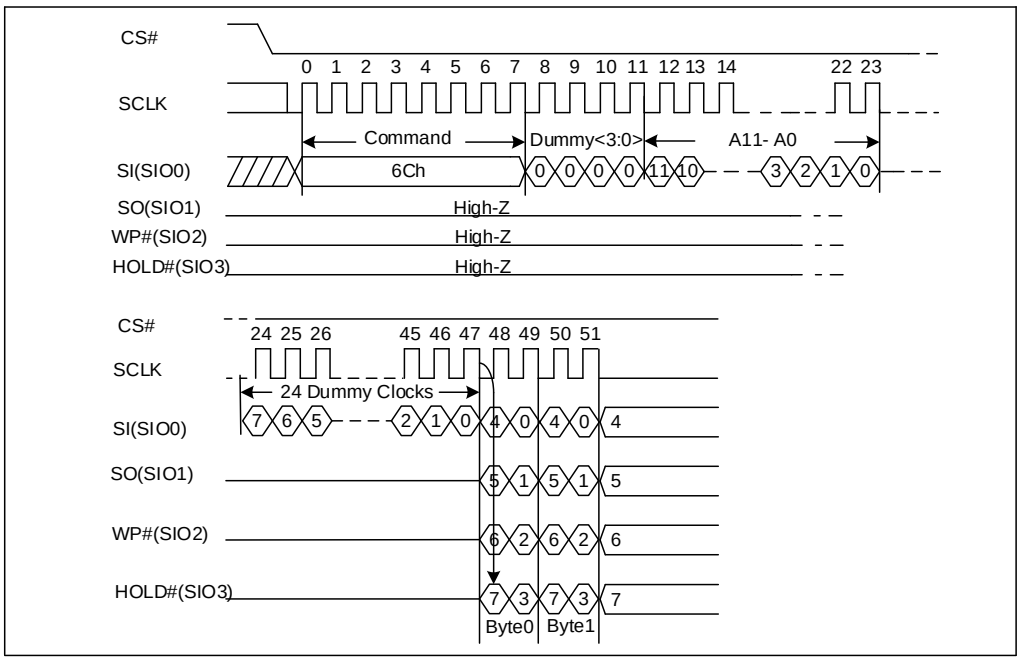


Figure 10-8.b Continuous Read Mode1 (NR=0, CRDC=0)

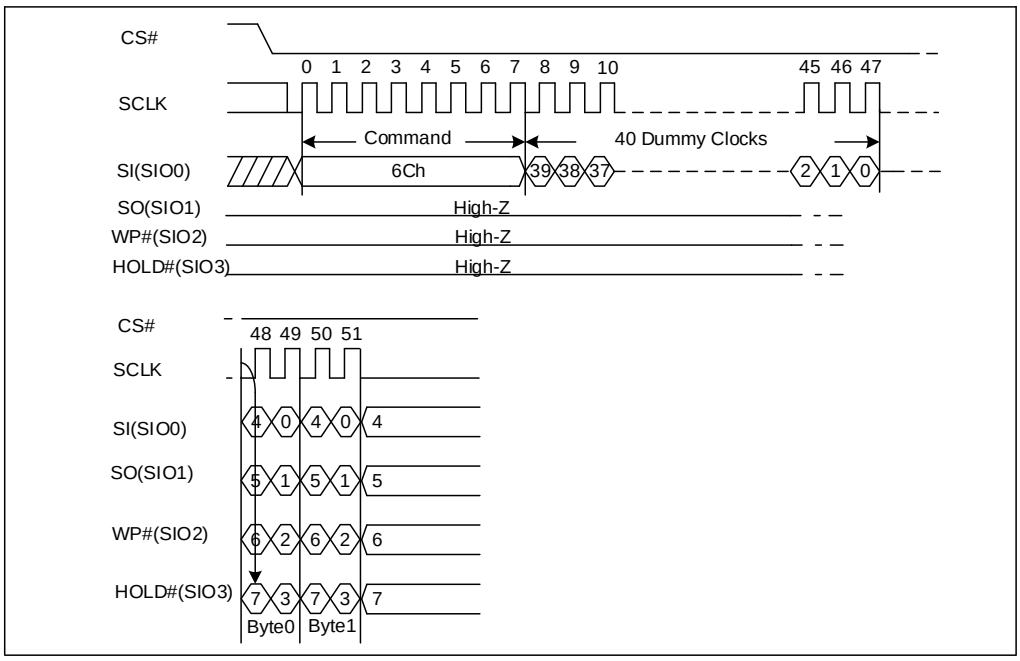
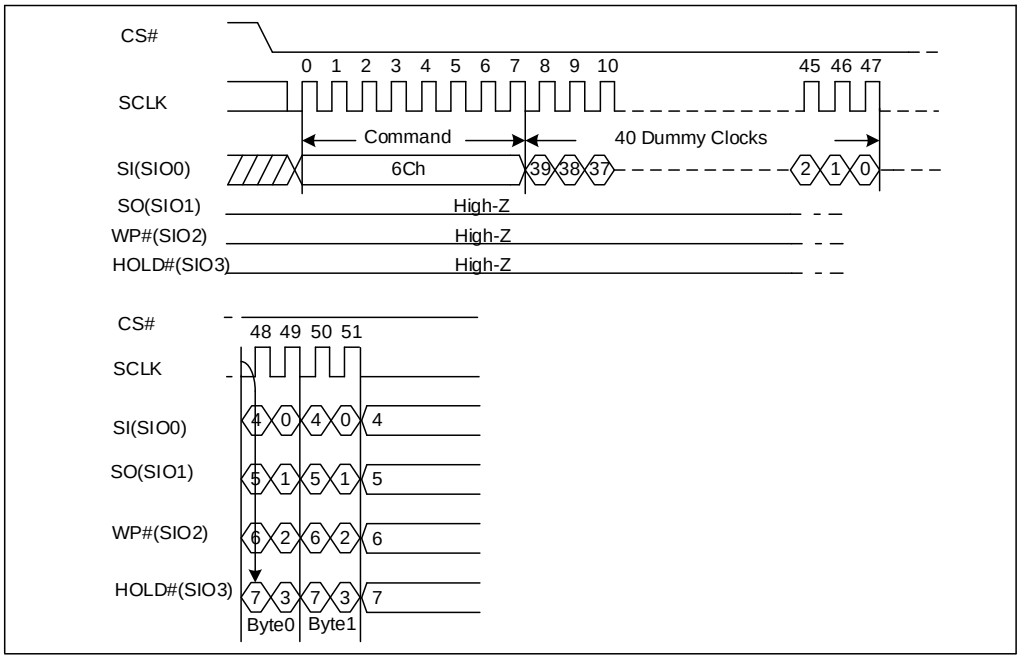


Figure 10-8.c Continuous Read Mode2 (NR=0, CRDC=1)



10.10 Read From Cache Dual IO (BBh)

The Read from Cache Dual I/O command (BBh) is similar to the Read form Cache x2 command (3Bh) but with the capability to input the 4 Dummy bits, followed by a 12-bit column address for the starting byte address and a dummy byte by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first address byte can be at any location. The address increments automatically to the next higher address after each byte of data shifted out until the boundary wrap bit.

DC bit can change the dummy byte in Normal Read Mode and Continuous Read Mode2 for high frequency. Please refer to the table 7-5.

Figure 10-9.a Normal Read (Default, NR=1, DC=0)

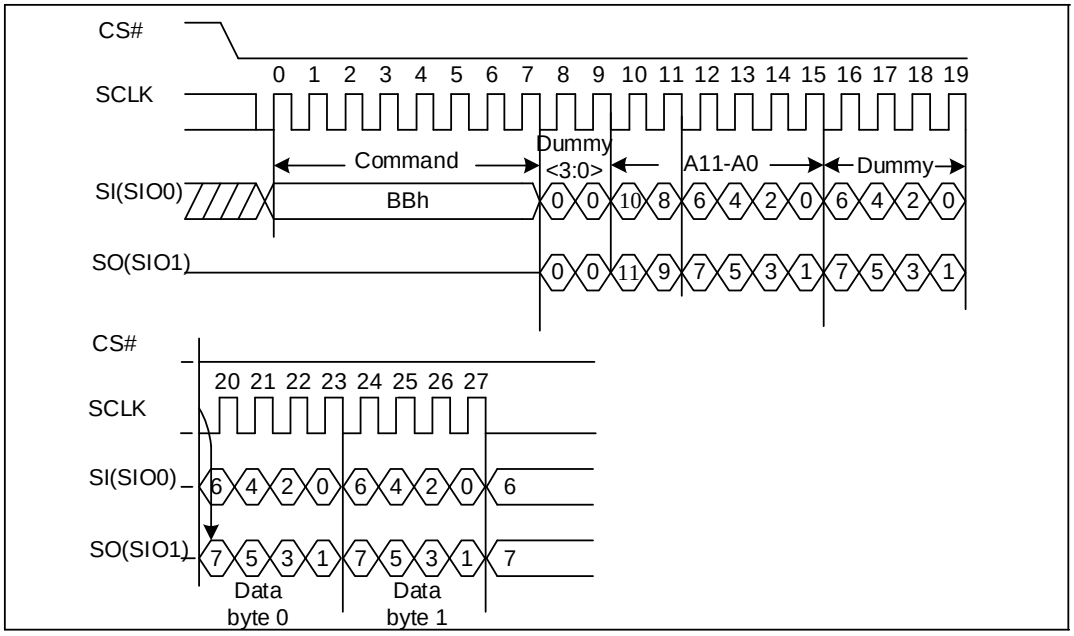


Figure 10-9.a Normal Read (NR=1, DC=1)

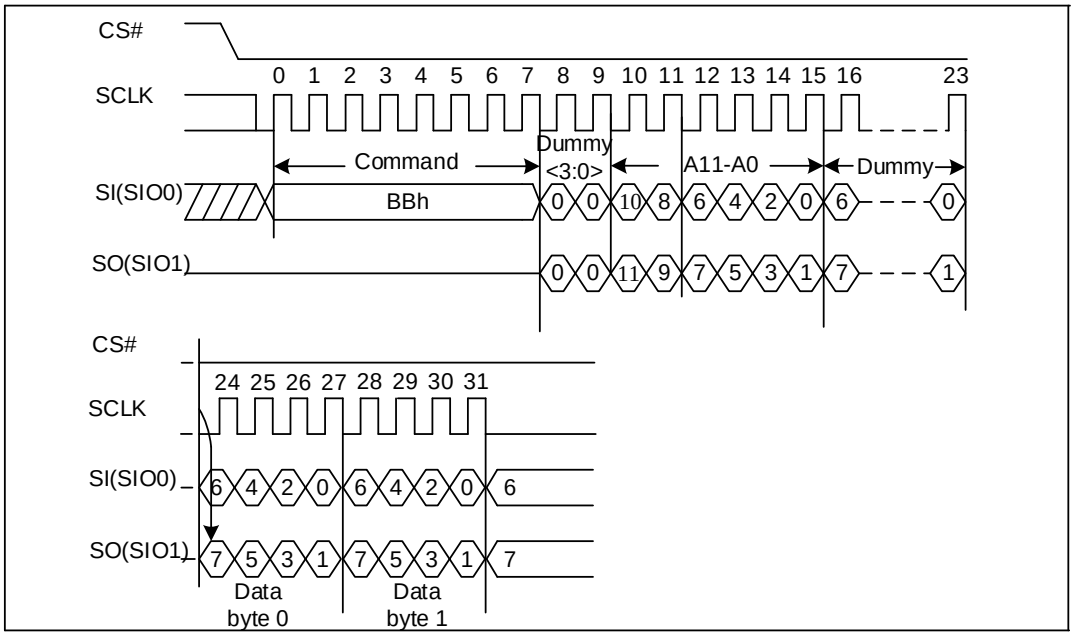


Figure 10-9.b Continuous Read Mode1 (NR=0, CRDC=0)

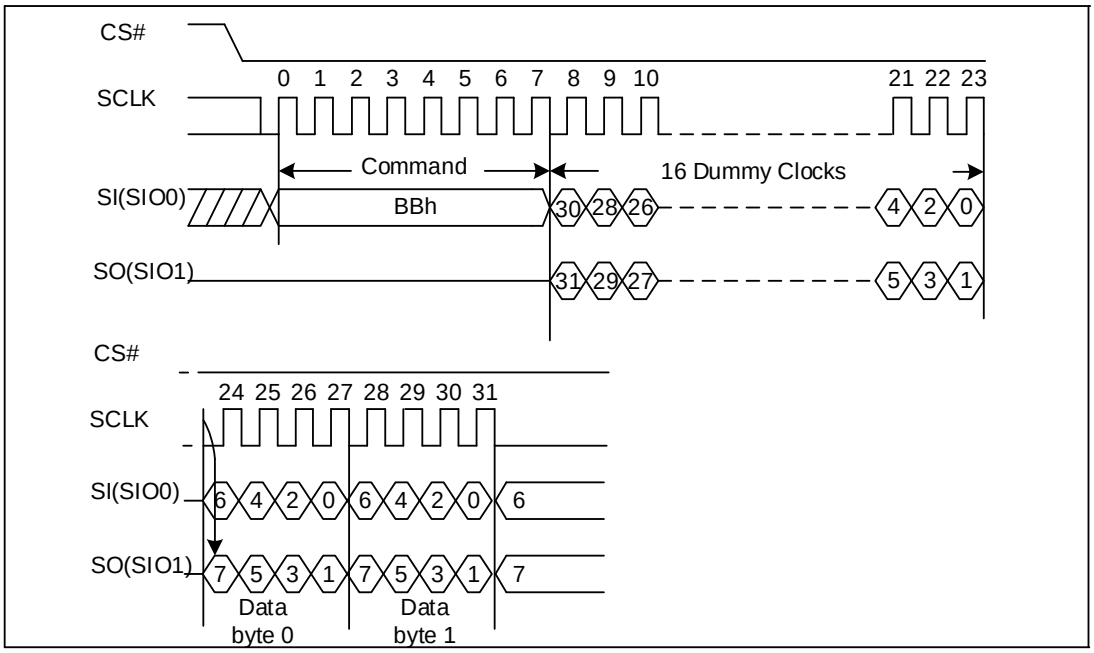


Figure 10-9.c Continuous Read Mode2 (NR=0, CRDC=1, DC=0)

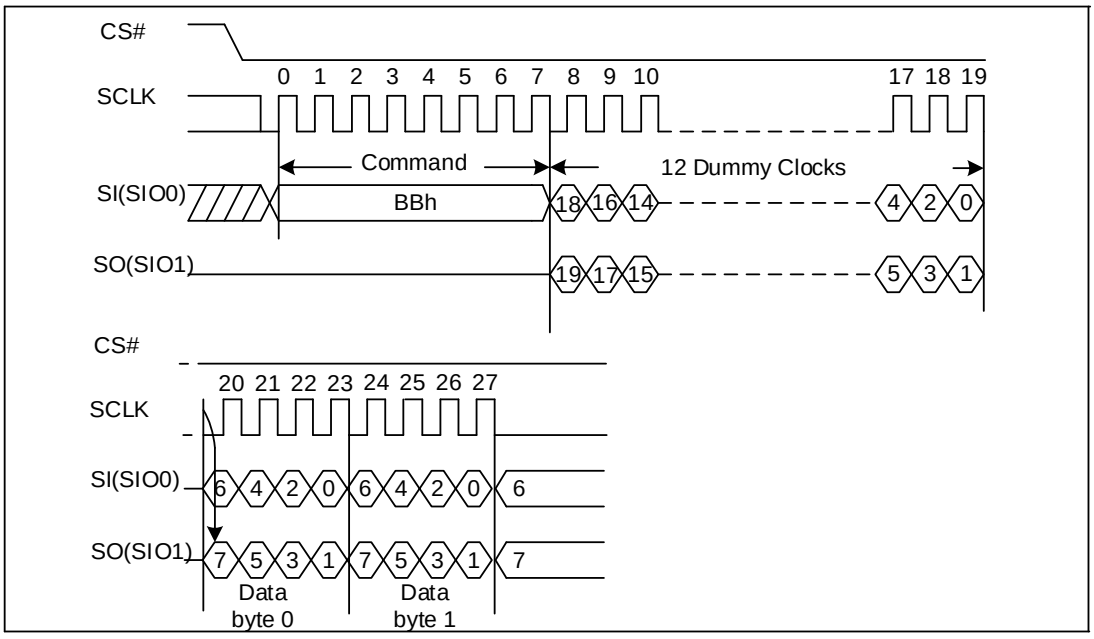
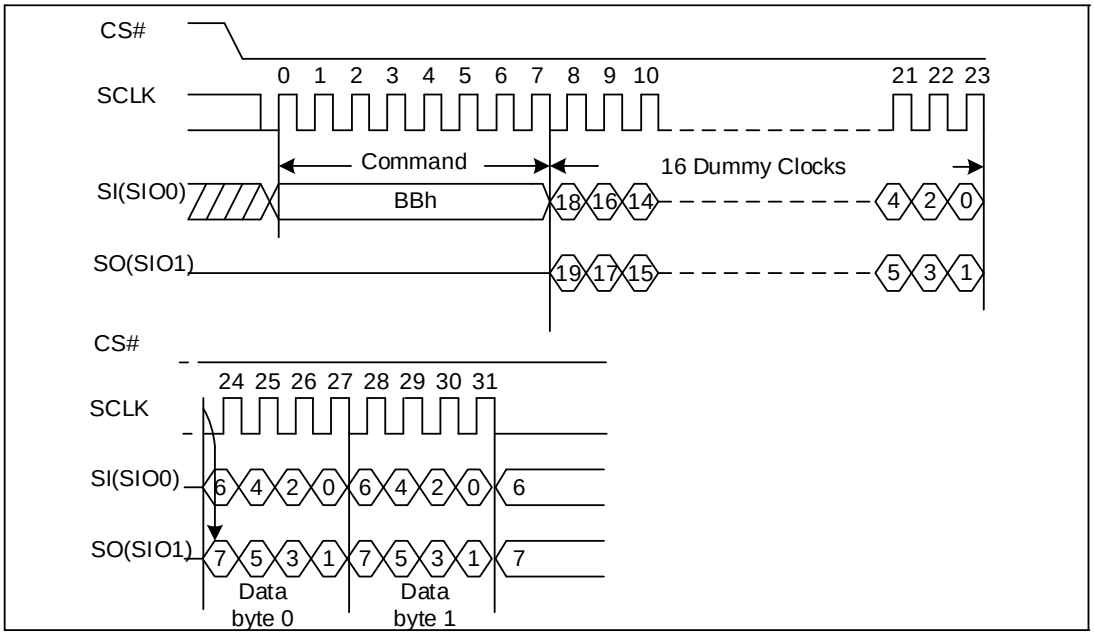


Figure 10-9.c Continuous Read Mode2 (NR=0, CRDC=1, DC=1)



10.11 Read From Cache Dual IO with 4-Byte Address (BCh)

Figure 10-10.a Normal Read (Default, NR=1)

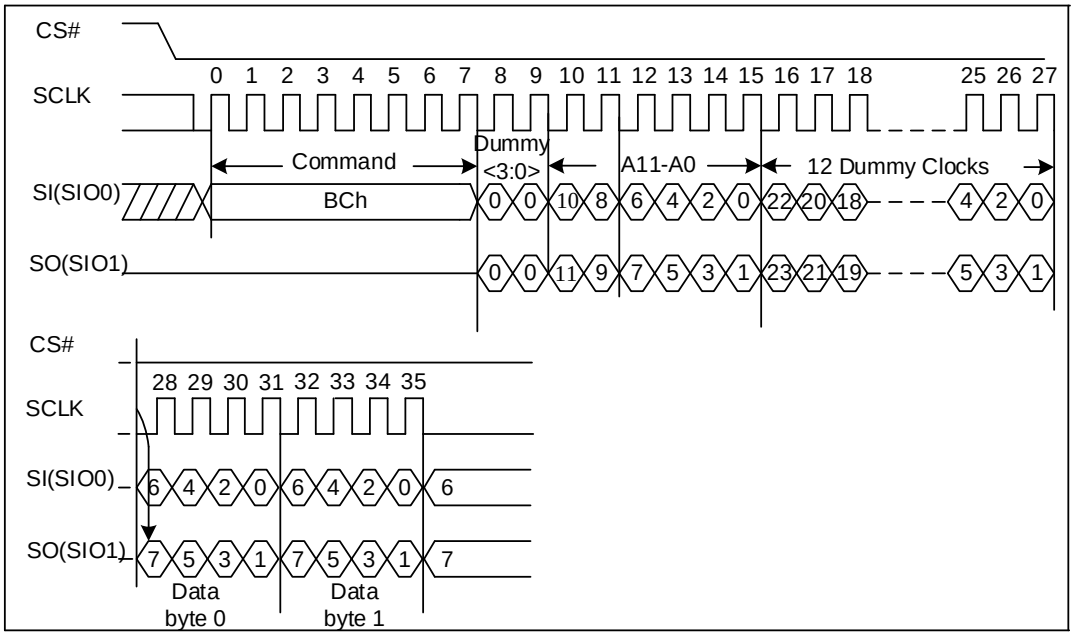


Figure 10-10.b Continuous Read Mode1 (NR=0, CRDC=0)

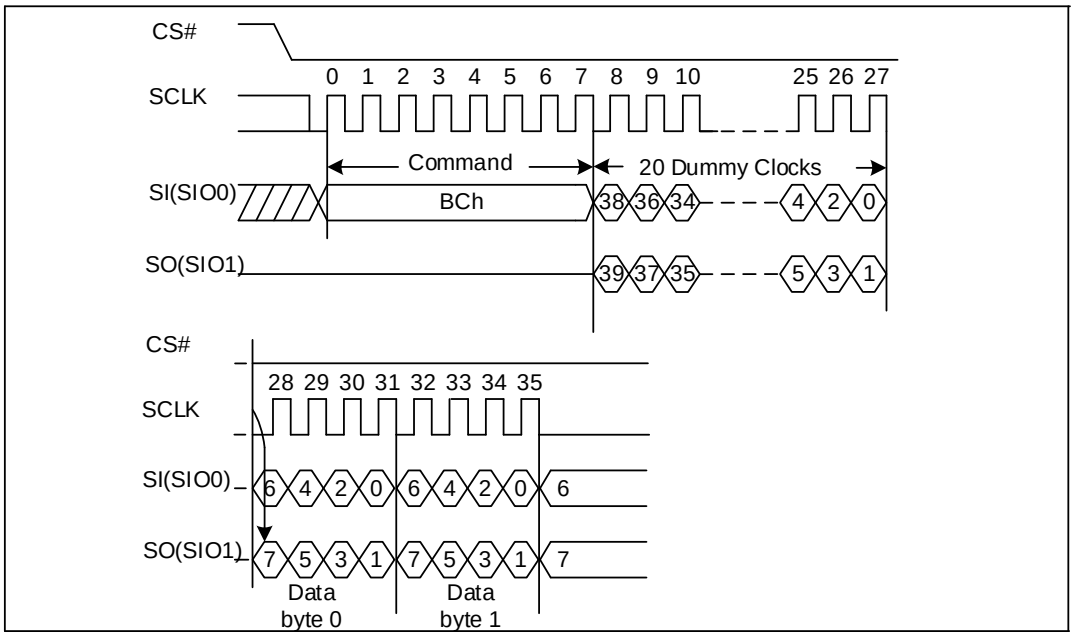
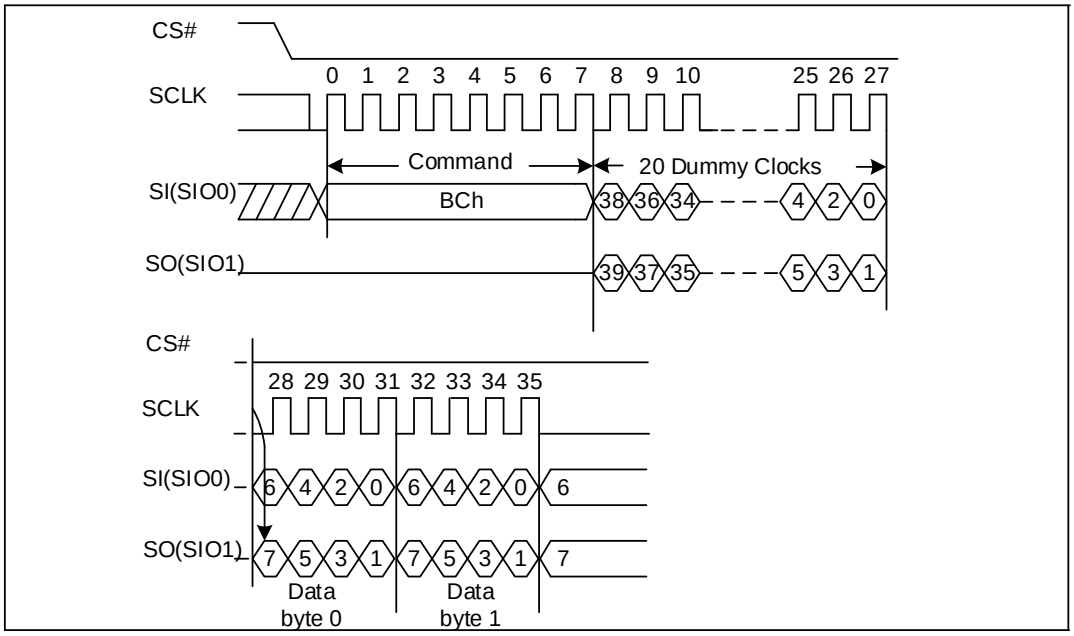


Figure 10-10.c Continuous Read Mode2 (NR=0, CRDC=1)



10.12 Read From Cache Quad IO (EBh)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command but with the capability to input the 4 dummy bits, followed a 12-bit column address for the starting byte address and a dummy byte by SIO0, SIO1, SIO2, SIO3, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the boundary wrap bit. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache quad IO command.

DC bit can change the dummy byte in Normal Read Mode and Continuous Read Mode2 for high frequency. Please refer to the table 7-5.

Figure 10-11.a Normal Read (Default, NR=1, DC=0)

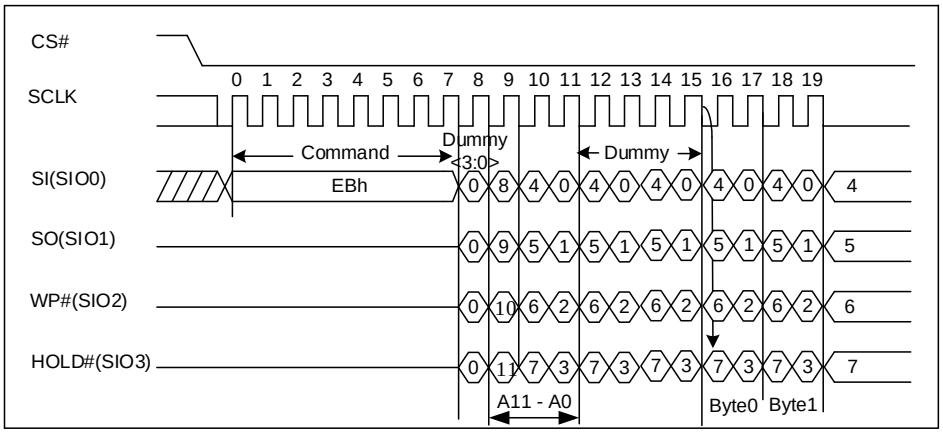


Figure 10-11.a Normal Read (NR=1, DC=1)

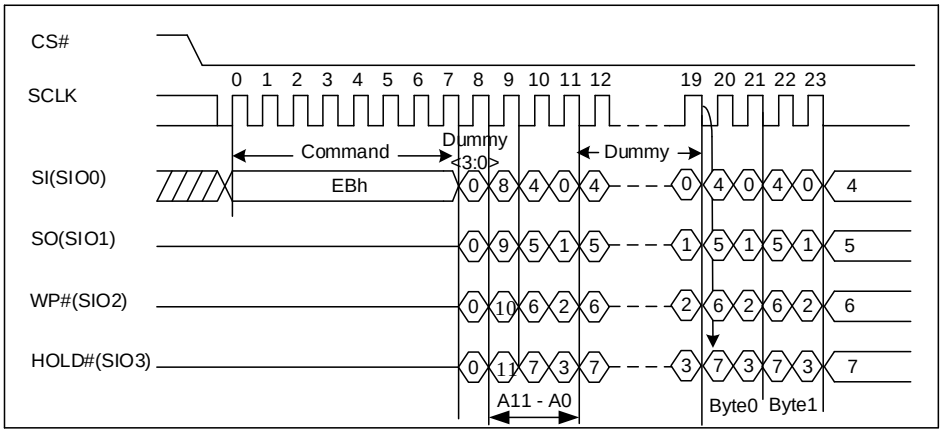


Figure 10-11.b Continuous Read Mode1 (NR=0, CRDC=0)

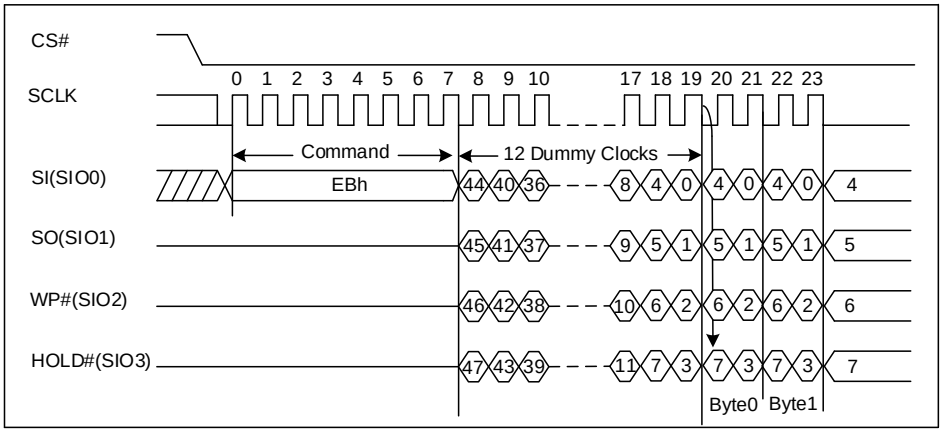


Figure 10-11.c Continuous Read Mode2 (NR=0, CRDC=1, DC=0)

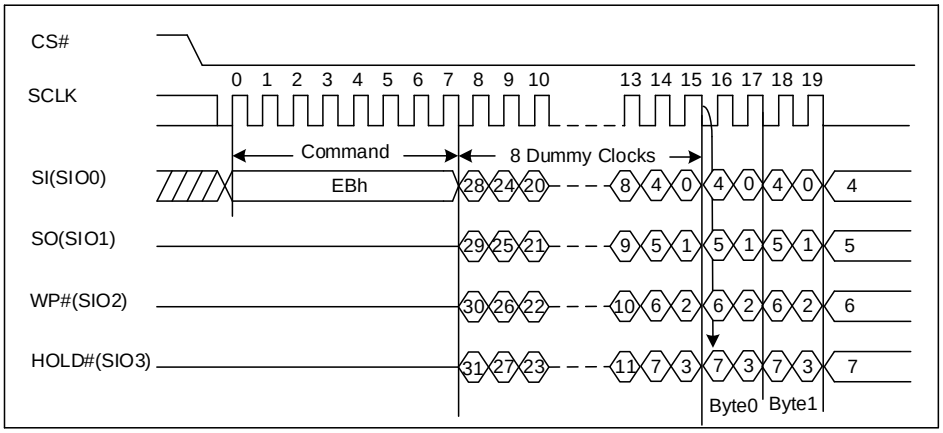
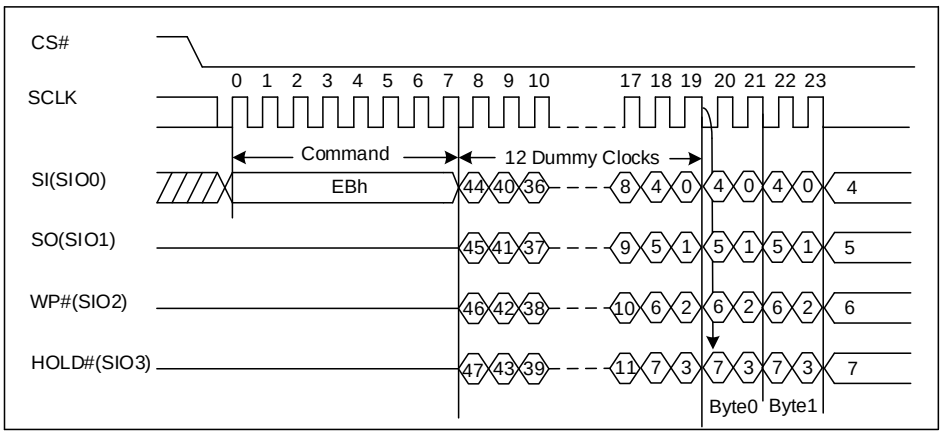


Figure 10-11.c Continuous Read Mode2 (NR=0, CRDC=1, DC=1)



10.13 Read From Cache Quad IO with 4-Byte Address (ECh)

Figure 10-12.a Normal Read (Default, NR=1)

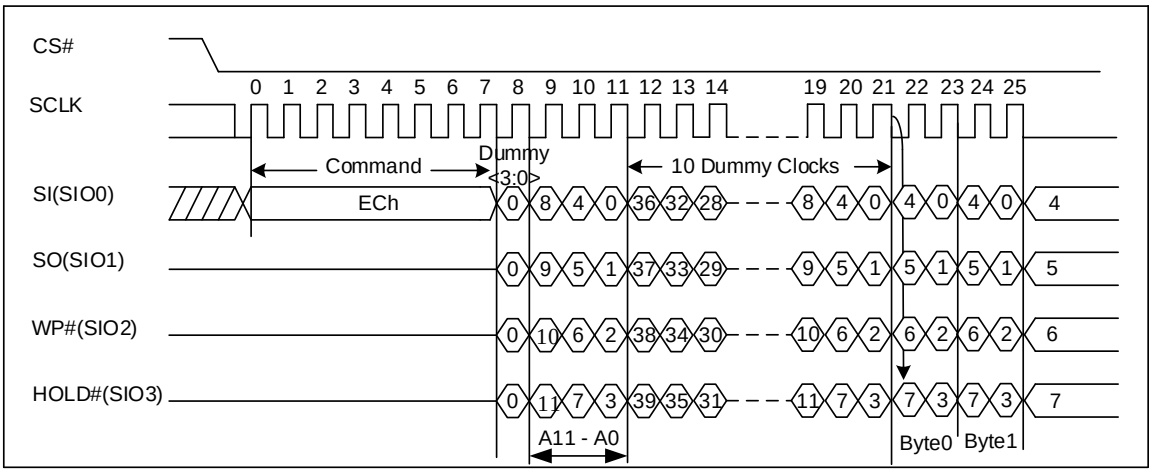


Figure 10-12.b Continuous Read Mode1 (NR=0, CRDC=0)

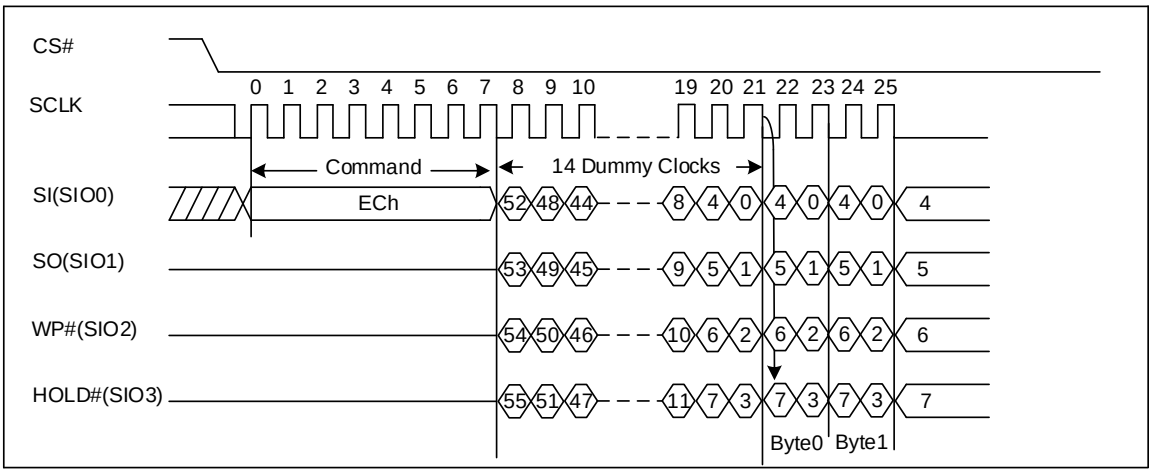
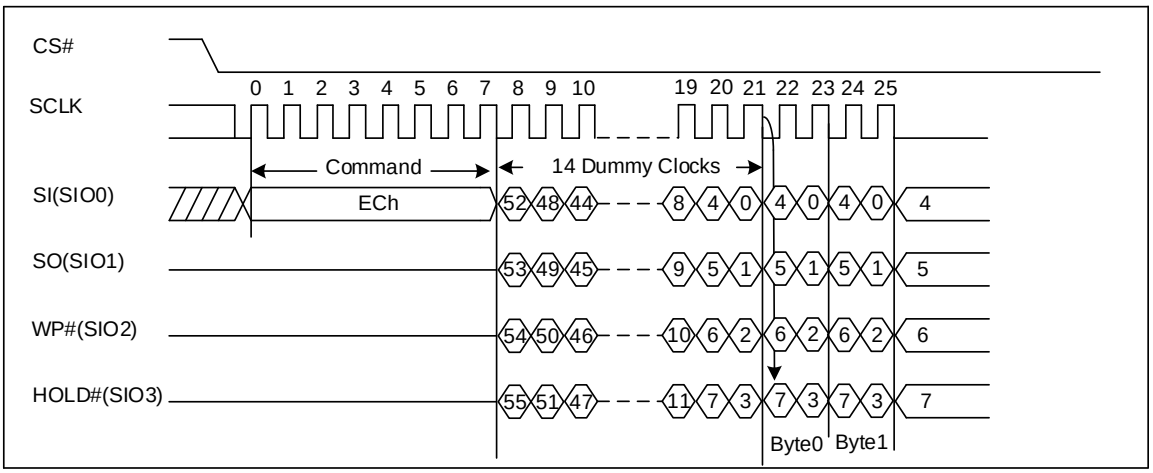


Figure 10-12.c Continuous Read Mode2 (NR=0, CRDC=1)



10.14 DTR Read From Cache Quad I/O with 4-Byte Address (EDh)

Figure 10-13.a Normal Read (Default, NR=1)

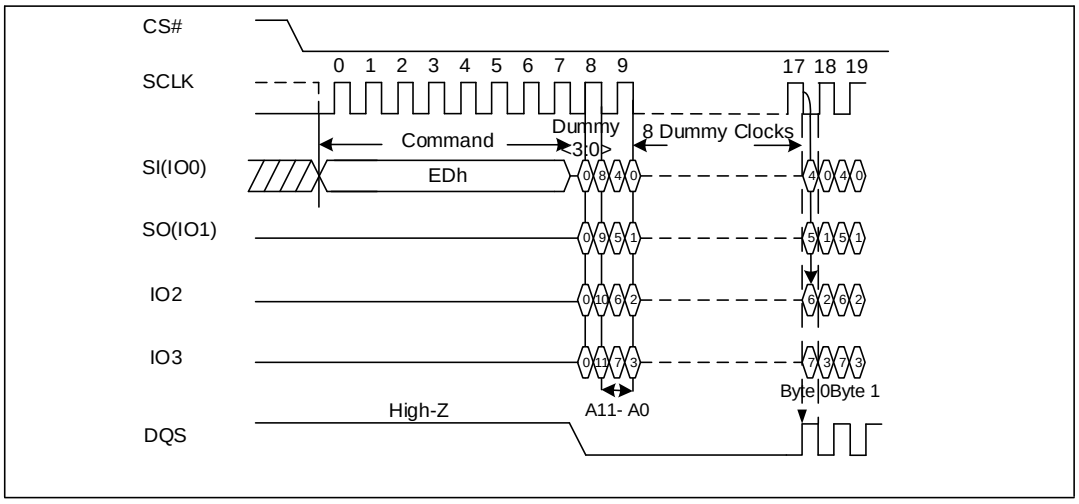


Figure 10-13.b Continuous Read Mode1 (NR=0, CRDC=0)

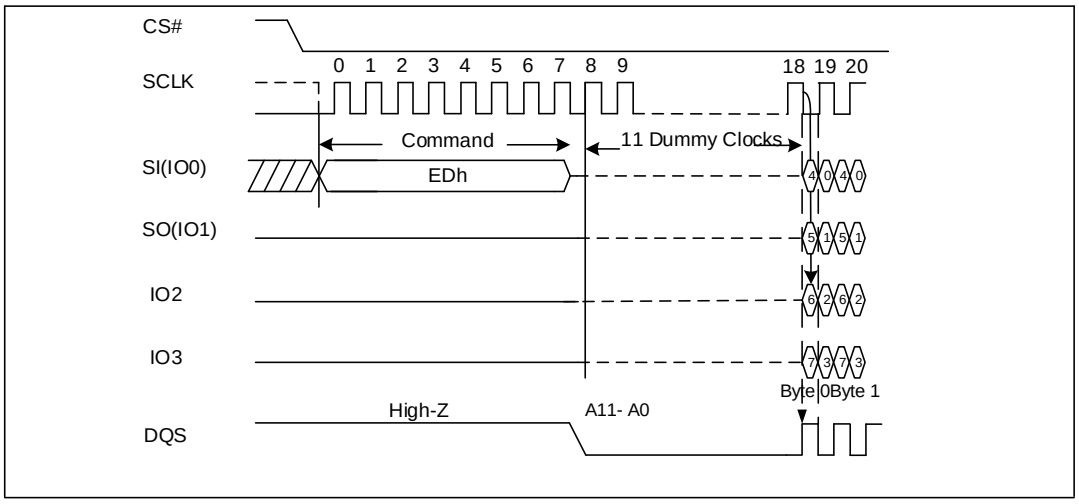
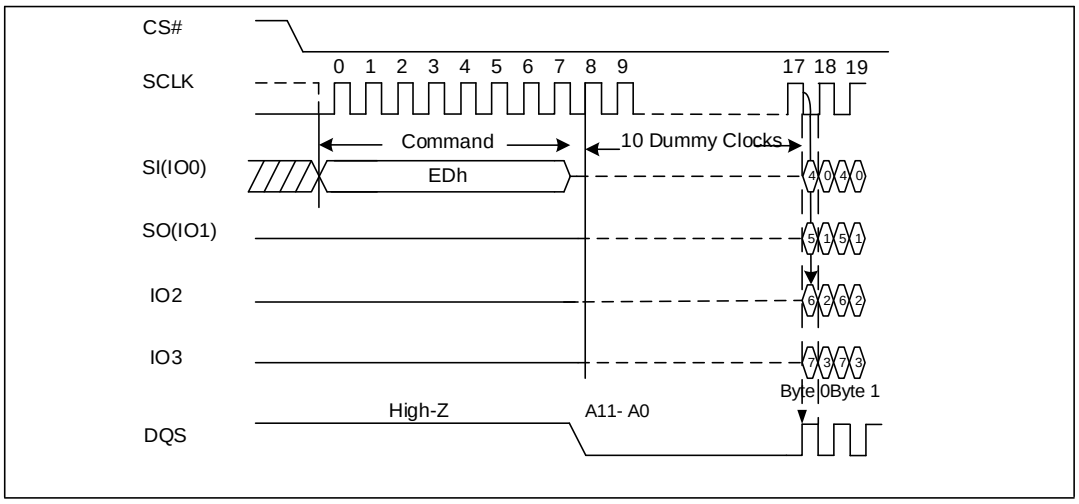


Figure 10-13.c Continuous Read Mode2 (NR=0, CRDC=1)



10.15 DTR Read From Cache Quad I/O (EEh)

The DTR Quad IO command enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the DTR Quad IO command. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock.

The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole page can be read out at a single DTR Quad IO command. The address counter rolls over to 0 when the highest address has been reached. Once writing DTR Quad IO command, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

Note:

Please contact GigaDevice when there is a need to use the EEh command for DTR.

Figure 10-14. a Normal Read (Default, NR=1)

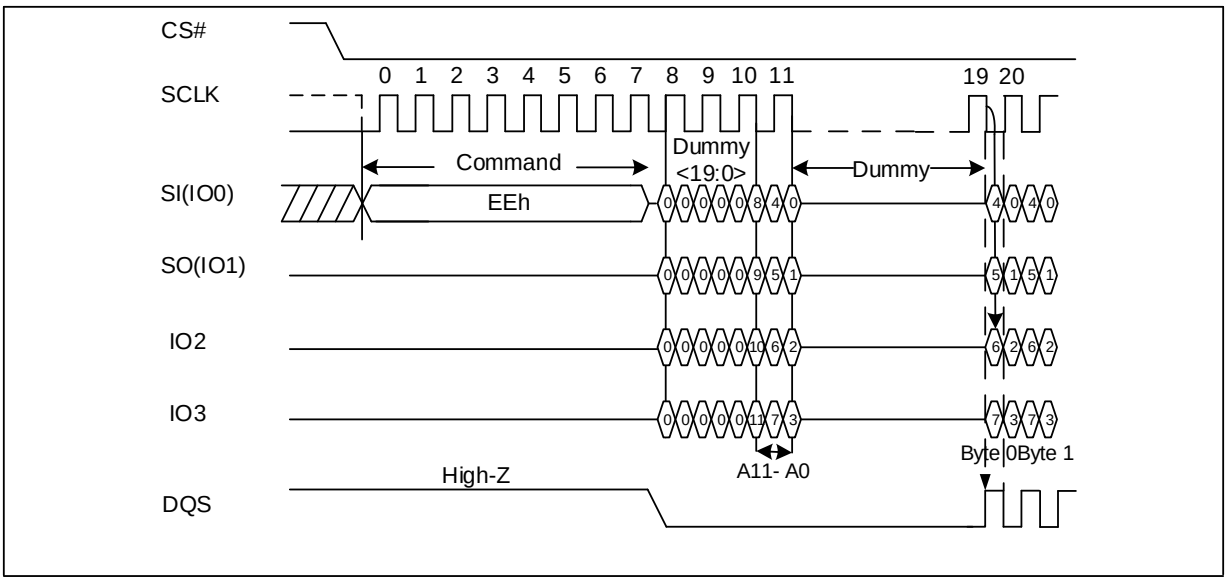


Figure 10-14. b Continuous Read Mode1 (NR=0, CRDC=0)

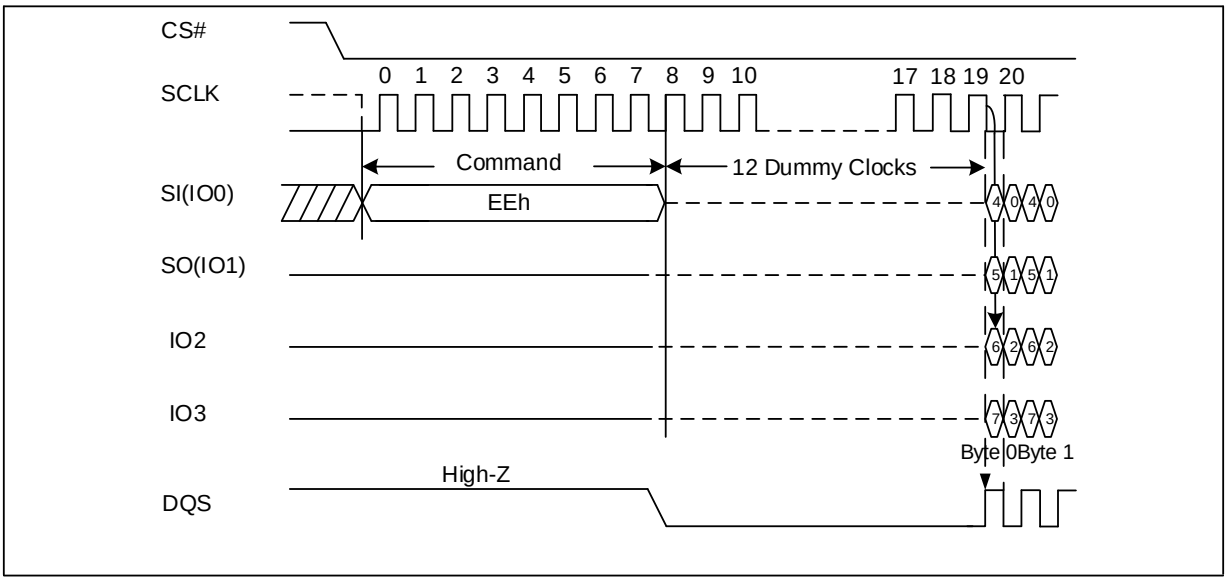
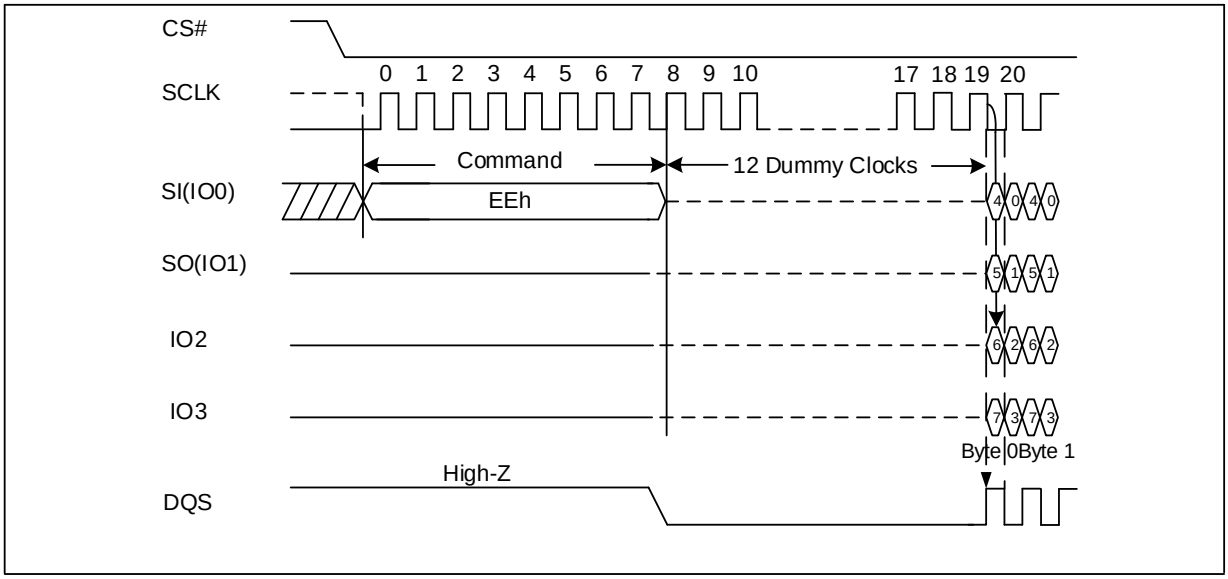


Figure 10-14.c Continuous Read Mode2 (NR=0, CRDC=1)



10.16 Cache Read Function (31h/30h/3Fh)

A “Cache Read” function has been implemented in SPI series to improve the overall read throughput. It is possible to transfer the data from array to the Data Register simultaneously while a Read Data command is being performed to read out data from the Cache Register.

When multiple pages of data is to be read out sequentially, the host should issue a “Page Read to Cache (13h)” command followed by a Page Address which specifies the starting page of the data (1). Once the command is accepted, the host should use “Get Feature (0Fh)” to check the OIP bit value to determine if the internal operation has completed or not.

Prior to issuing a Read Data command to read out the data in the Cache Register, the host can issue a “Next Page Cache Read (31h)” command to initiate the Cache Read operation. There is not necessary to provide any Page Address since the device will automatically increment the Page Address specified earlier by “Page Read to Cache (13h)” instruction. After the “Next Page Cache Read” (31h) command issued, the device starts to transfer data from Data Register to Cache Register for tCBSYR. After tCBSYR, CBSY bit (through GET FEATURE command to check this status bit) goes to 1 from 0.

While the device is transferring the next page array data to the Data Register, the host can now use Read From Cache command to shift out the current page data inside the Cache Register. Once CBSY bit becomes 0, the host can issue a Read Data command to shift out the Cache Register data, then issue “Next Page Cache Read (31h)” again to read the next page in the array.

If the current page address is the last page of the data being read out, the host should issue “Last Page Cache Read (3Fh)” instead of “Next Page Cache Read (31h)”, and proceed with the last Read from cache command.

Table 10-1 Cache Read instruction description

Instruction	Command Code	Description
Next Page Cache Read Sequential	31h	Issue prior to current page “Read From Cache” and read next page data into Data Register
Next Page Cache Read Random	30h+addr	Issue prior to current page “Read From Cache” and read special page data into Data Register
Last Page Cache Read	3Fh	Issue prior to last page “Read From Cache” at the end of a block or the end of the data being read

Notes:

1. Upon powered up, SPI NAND will automatically load Block-0/Page-0 data into the Cache Register. If this is the starting page of the data that is to be read out, it is not necessary to issue a “Page Read to Cache (13h)” command to initiate the “Cache Read” operation.
2. Before issuing 31h/30h/3Fh, CBSY bit must be checked to make sure CBSY=0, device is not performing any internal operations.
3. The Cache Read Operation is only available in Normal Read Mode.

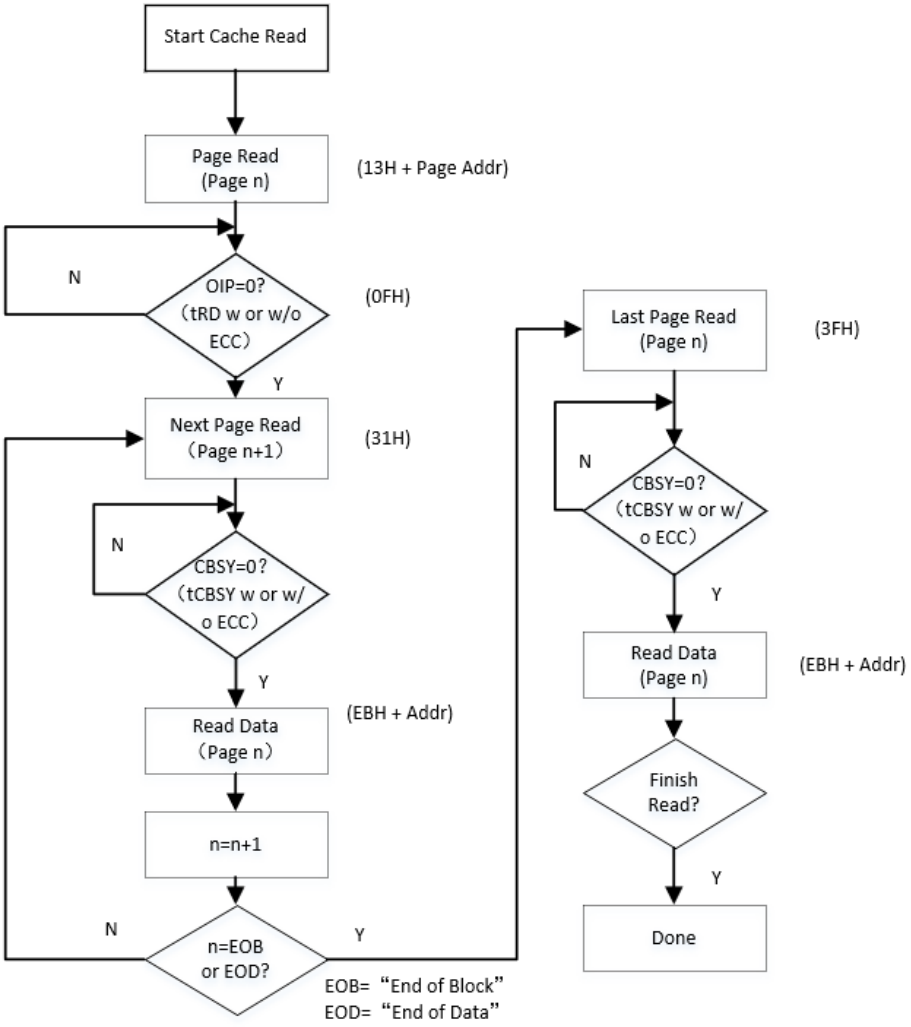
The command sequence is as follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURES command to read the status until OIP status bit is changed from 1 to 0)
- 31h (NEXT PAGE CACHE READ command to transfer data from data register to cache register and kick off the next page transfer from array to data register)
- 0Fh (GET FEATURES command to read the status until CBSY=0)
- 03h/0Bh/0Ch/3B/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh (Read From Cache command)
- 3Fh (LAST PAGE CACHE READ command to end the read page cache sequence and copy a last page from the data register to cache register)
- 0Fh (GET FEATURES command to read the status until CBSY=0)
- 03h/0Bh/0Ch/3B/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh (Read From Cache command)

Note：

1. Read From Cache command is available to read out the data in the Cache Register.
2. For high speed performance, we recommend to use Quad IO to read out the data in the Cache Register.
3. The Cache Read Function is only available in Normal Read Mode.

Figure 10-15. Cache Read operation flow chart



Example command sequence with one block data Cache Read:

Current Page Addr	Page/Cache Read	Read Data	Time
0	Page Read (13h + Pg Addr 0)		Wait tRD
0	Next Pg. Cache Rd. (31h)	Read Data (Page 0)	tCBSYR
1	Next Pg. Cache Rd. (31h)	Read Data (Page 1)	tCBSYR
2	Next Pg. Cache Rd. (31h)	Read Data (Page 2)	tCBSYR
…			
…			
62	Next Pg. Cache Rd. (31h)	Read Data (Page 62)	tCBSYR
63	Last Pg. Cache Rd. (3Fh)	Read Data (Page 63)	tOUTPUT

Figure 10-16. Page Read to cache Sequence Diagram

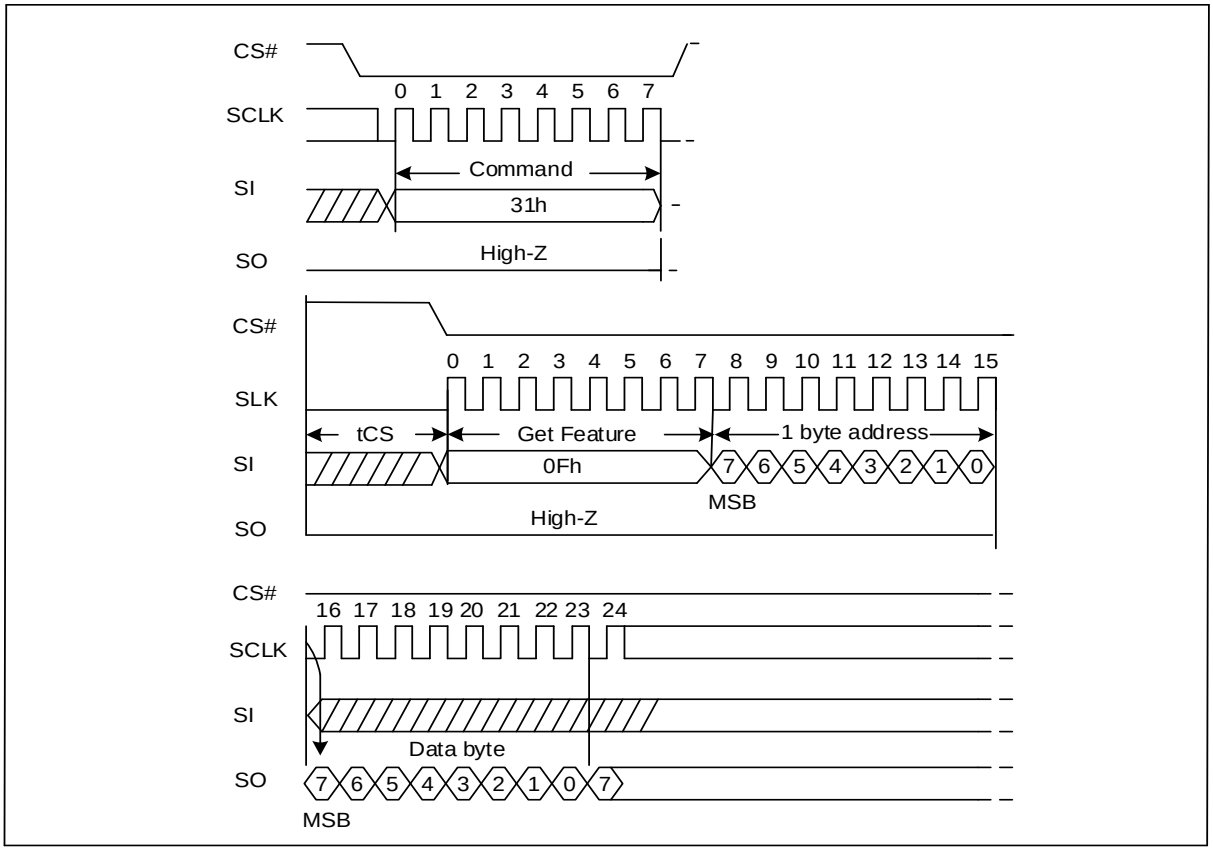


Figure 10-17. Page Read to cache Random Diagram

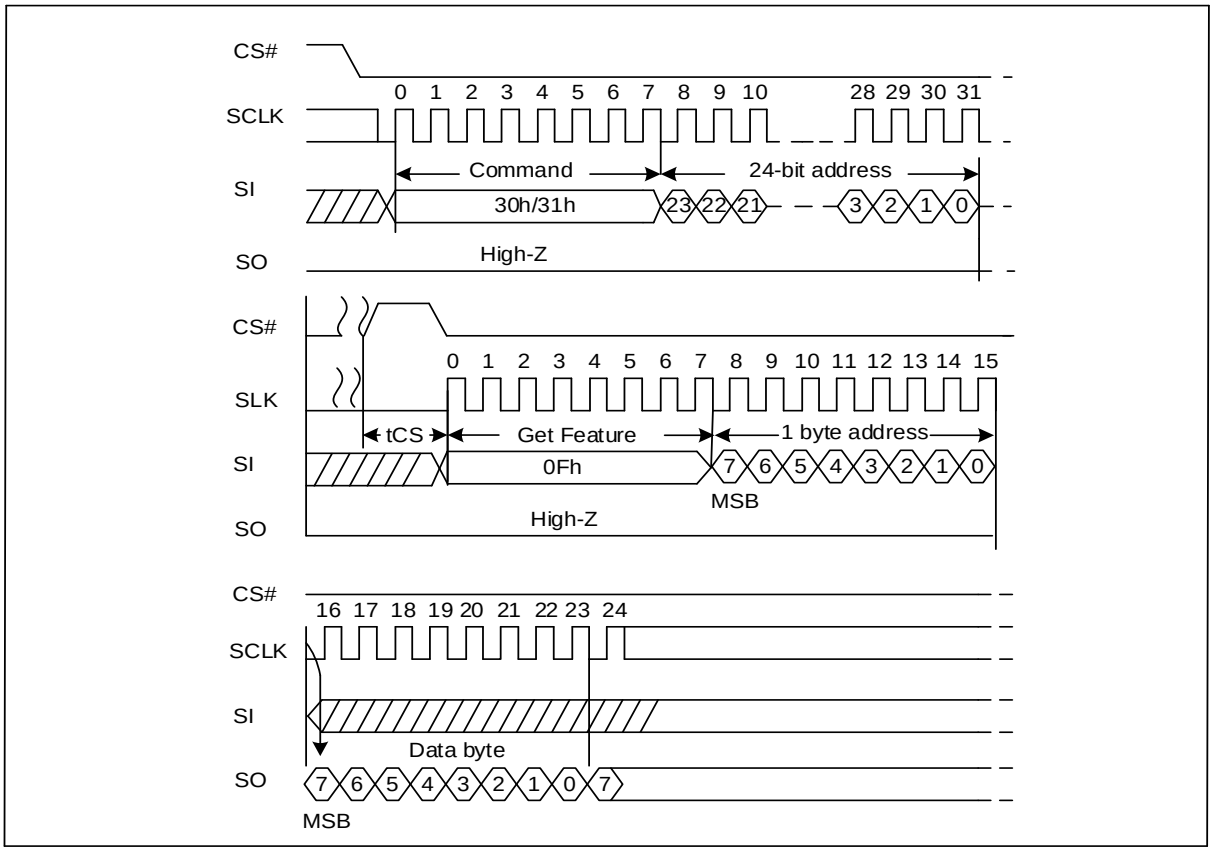


Figure 10-18. Page Read to cache Sequence Diagram

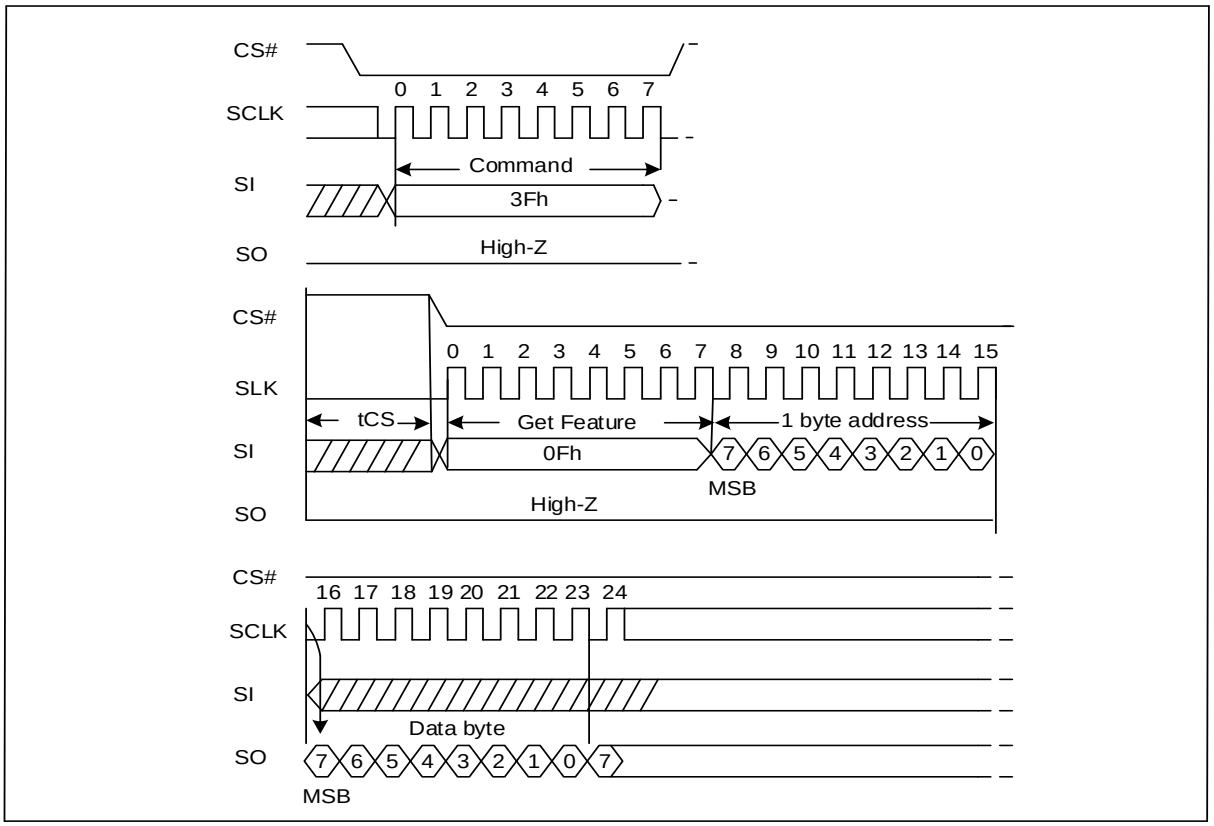
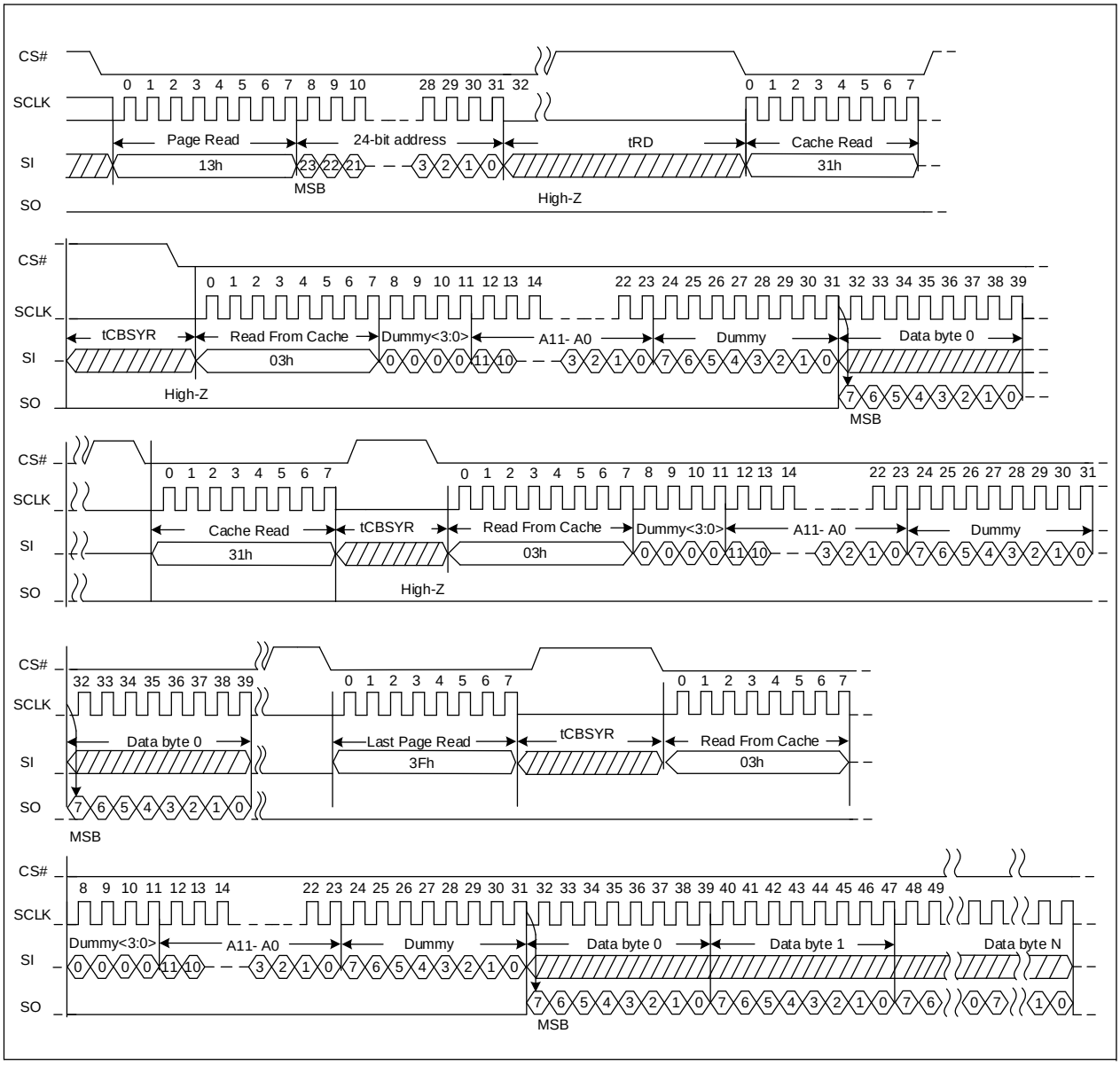


Figure 10-19. Page Read to Cache Timing Diagram



10.17 Read ID (9Fh)

The READ ID command is used to identify the NAND Flash device.

• The READ ID command outputs the Manufacturer ID and Device ID. See Table for details.

Figure 10-20. Read ID Sequence Diagram

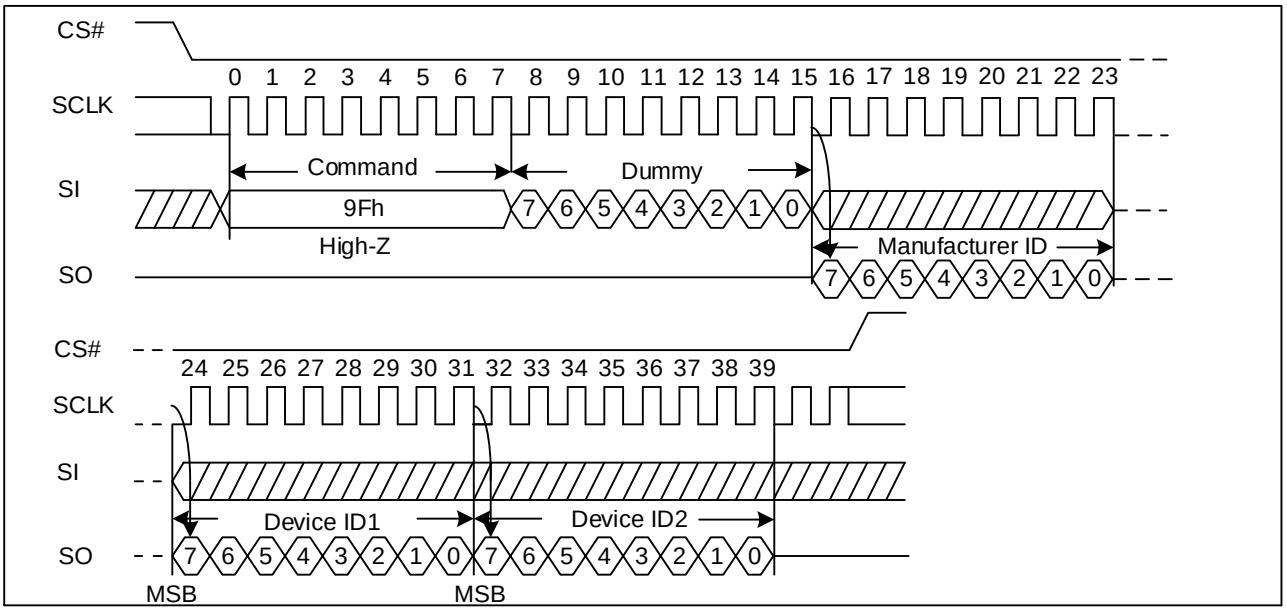


Table 10.2 READ ID Table

Part No	MID	DID1	DID2
GD5F1GM9UE	C8h	91h	01h
GD5F1GM9RE	C8h	81h	01h

10.18 Read UID

The Read Unique ID function is used to retrieve the 16-byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement are stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

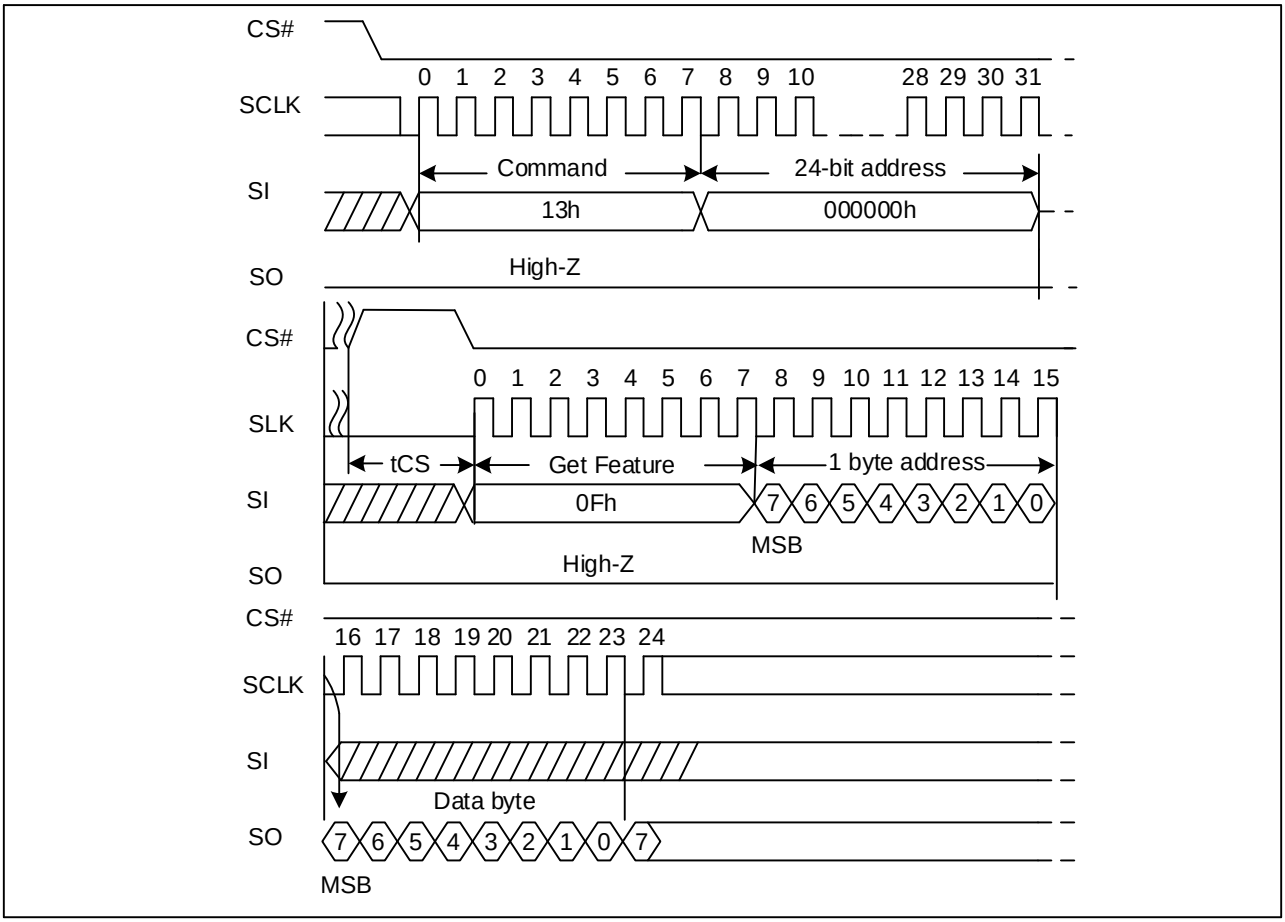
Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use page read to cache (13h) command with address 24'h000000h, read data from array to cache.
4. Use 0Fh (GET FEATURES command) read the status.
5. User can use Read from cache command(03h/0Bh), read 16 bytes UID from cache.
6. Use Set Feature command to set B0 register, to disable OTP_EN, to exit OTP mode.

Note：

1. In OTP Mode (OTP_EN enabled), the Read from Cache command (03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh) has the same format as normal read mode. The NR bit can't influence the OTP mode (OTP_EN enabled).
2. Please don't exit OTP mode when reading UID, Parameter Page, CASN Page.

Figure 10-21. Read UID to cache and Get Feature command Sequence Diagram



10.19 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. The whole data structure is repeated at least three times. The Read from Cache command can be issued during execution of the read parameter page to read specific portion-soft the parameter page.

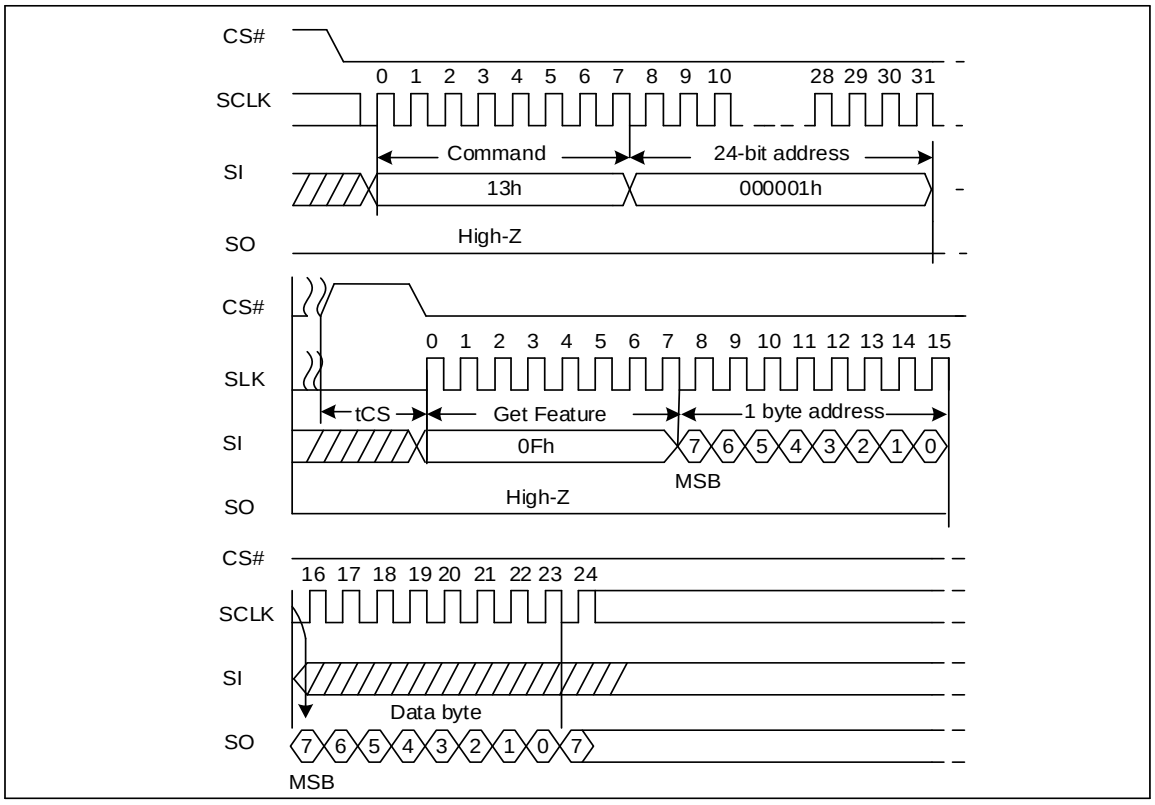
Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 24'h000001h. Load parameter page from array to cache.
4. Use 0Fh (GET FEATURES command) read the status
5. User can use Read from cache command (03h/0Bh), read parameter page from cache from Byte0 to Byte767.
6. Use Set Feature command to set B0 register, to disable OTP_EN, to exit OTP mode.

Note：

1. In OTP Mode (OTP_EN enabled), the Read from Cache command (03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh) has the same format as normal read mode. The NR bit can't influence the OTP mode (OTP_EN enabled).
2. Please don't exit OTP mode when reading UID, Parameter Page, CASN Page.

Figure 10-22. Read parameter page to cache and Get Feature command Sequence Diagram



Parameter page table as follow (1G)

Byte	O/M	Description	3.3V/1.8V
0-3	M	Parameter page signature Byte 0: 4FH, “O” Byte 1: 4EH, “N” Byte 2: 46H, “F” Byte 3: 49H, “I”	4FH 4EH 46H 49H
4-5	M	Revision number 0-15 Reserved (0)	00h 00h
6-7	M	Features supported 0-15 Reserved (0)	00h 00h
8-9	M	Reserved (0)	00h 00h
10-31		Reserved (0)	00h … 00h
		Manufacturer Information block	
32-43	M	Device manufacturer (12 ASCII characters)“GIGADEVICE ”	47h 49h 47h 41h 44h 45h 56h 49h 43h 45h 20h 20h
44-63	M	Device model (20 ASCII characters) **Device Model** | **ORGANIZATION** | **VCC RANGE** “GD5F1GM9U” | X4 | 2.7v ~ 3.6v “GD5F1GM9R” | X4 | 1.7v ~ 2.0v	47h 44h 35h 46h 31h 47h 4Dh 39h 55h/52h 20h 20h 20h 20h 20h 20h

			20h 20h 20h 20h 20h
64	M	JEDEC manufacturer ID“C8”	C8h
65-66	O	Date code	00h 00h
67-79		Reserved	00h 00h 00h
		Memory organization block	
80-83	M	Number of data bytes per page	00h 08h 00h 00h
84-85	M	Number of spare bytes per page	80h 00h
86-89	M	Number of data bytes per partial page	00h 02h 00h 00h
90-91	M	Number of spare bytes per partial page	20h 00h
92-95	M	Number of pages per block	40h 00h 00h 00h
96-99	M	Number of blocks per logical unit (LUN)	00h 04h 00h 00h
100	M	Number of logical units (LUNs)	01h
101	M	Reserved	00h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum	14h 00h
105-106	M	Block endurance	08h 04h
107	M	Guaranteed valid blocks at beginning of target	08h
108-109	M	Block endurance for guaranteed valid blocks	00h 00h

110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	00h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00h
115-127		Reserved	00h … 00h
		Electrical parameters block	
128	M	I/O capacitance	08h
129-130	M	IO clock support	00h 00h
131-132	O	Reserved (0)	00h 00h
133-134	M	tPROG Maximum page program time (us)	58h 02h
135-136	M	tBERS Maximum block erase time (us)	10h 27h
137-138	M	tR Maximum page read time (us)	96h 00h
139-140	M	Reserved	00h 00h
141-163		Reserved	00h
		Vendor block	
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255	M	Integrity CRC	Set on test
		Redundant parameter pages	
256-511	M	Value of bytes 0-255	
512-767	M	Value of bytes 0-255	

Notes:

1. “O” Stands for Optional, “M” for Mandatory
2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details. The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X^{16} + X^{15} + X^2 + 1$， This polynomial in hex may be represented as 8005h.

3．The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Device Model	ORGANIZATION	VCC RANGE	CRC value B254/B255
“GD5F1GM9U”	X4	2.7v ~ 3.6v	D2h/F4h
“GD5F1GM9R”	X4	1.7v ~ 2.0v	0Ah/39h

10.20 Read CASN Page

The Read CASN Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. The whole data structure is repeated at least three times.

Sequence is as follows (Same as Read Parameter Page):

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 24'h000001h. Load parameter page and CASN page from array to cache.
4. Use 0Fh (GET FEATURES command) read the status
5. User can use Read from cache command (03h/0Bh), read CASN page from Byte768 to Byte1023.
6. Use Set Feature command to set B0 register, to disable OTP_EN, to exit OTP mode.

Note：

1. In OTP Mode (OTP_EN enabled), the Read from Cache command (03h/0Bh/0Ch/3Bh/3Ch/6Bh/6Ch/BBh/BCh/EBh/ECh/EDh/EEh) has the same format as normal read mode. The NR bit can't influence the OTP mode (OTP_EN enabled).
2. Please don't exit OTP mode when reading UID, Parameter Page, CASN Page.

CASN page table as follow

Byte	Description	3.3V	1.8V
768-771	CASN page signature Byte 0: 43h, "C" Byte 1: 41h, "A" Byte 2: 53h, "S" Byte 3: 4Eh, "N"	 43h 41h 53h 4Eh	 43h 41h 53h 4Eh
772	Revision number bit7~4: major version, bit3~0: minor version	10h	10h
773-785	Device manufacturer (13 ASCII characters) "GIGADEVICE "	47h 49h 47h 41h 44h 45h 56h 49h 43h 45h 20h 20h 20h	47h 49h 47h 41h 44h 45h 56h 49h 43h 45h 20h 20h 20h

786-801	Device model (16 ASCII characters) “GD5F1GM9UE” “GD5F1GM9RE”		47h 44h 35h 46h 31h 47h 4Dh 39h 55h 45h 20h 20h 20h 20h 20h 20h	47h 44h 35h 46h 31h 47h 4Dh 39h 52h 45h 20h 20h 20h 20h 20h 20h
802-805	NAND Memory Organization	bit per cell 1: SLC 2: MLC	00h 00h 00h 01h	00h 00h 00h 01h
806-809		page size(2KB)	00h 00h 08h 00h	00h 00h 08h 00h
810-813		oob size (physical) (128B)	00h 00h 00h 80h	00h 00h 00h 80h
814-817		pages per block	00h 00h 00h 40h	00h 00h 00h 40h
818-821		eraseblock per lun	00h 00h 04h 00h	00h 00h 04h 00h
822-825		max bad blocks per lun	00h 00h 00h 14h	00h 00h 00h 14h
826-829		logical planes per	00h 00h 00h 01h	00h 00h 00h 01h

830-833		luns per target	00h 00h 00h 01h	00h 00h 00h 01h
834-837		total targets logic	00h 00h 00h 01h	00h 00h 00h 01h
838-841	ECC requirement	ECC strength (decimal)	00h 00h 00h 08h	00h 00h 00h 08h
842-845		ECC step size (decimal)	00h 00h 02h 00h	00h 00h 02h 00h
846	Flags: bit7: ECC algorithm (0: hamming, 1: BCH) bit6: ECC parity readable (0: no, 1: yes) bit5: support advanced ECC status (0: no, 1: yes) bit4: Support legacy ECC status (0: no, 1: yes) bit3: support on-die ECC (0: no, 1: yes) bit2: support continuous read (0: no, 1: yes) bit1: has continuous read feature bit (0: no, 1: yes) bit0: has quad mode bit (0: no, 1: yes)		EFh	EFh
847	Reserved		00h	00h
848	SDR read ability- Continuous read bit7: 1_8_8 continuous read (0: no, 1: yes) bit6: 1_1_8 continuous read (0: no, 1: yes) bit5: 1_4_4 continuous read (0: no, 1: yes) bit4: 1_1_4 continuous read (0: no, 1: yes) bit3: 1_2_2 continuous read (0: no, 1: yes) bit2: 1_1_2 continuous read (0: no, 1: yes) bit1: 1_1_1 fast continuous read (0: no, 1: yes) bit0: 1_1_1 continuous read (0: no, 1: yes)		3Fh	3Fh
849	SDR read ability- Non-continuous read bit7: 1_8_8 (0: no, 1: yes) bit6: 1_1_8 (0: no, 1: yes) bit5: 1_4_4 (0: no, 1: yes) bit4: 1_1_4 (0: no, 1: yes) bit3: 1_2_2 (0: no, 1: yes) bit2: 1_1_2 (0: no, 1: yes) bit1: 1_1_1 fast (0: no, 1: yes) bit0: 1_1_1 (0: no, 1: yes)		3Fh	3Fh

850	SDR 1_1_1 read	cmd	03h	03h
851		bit7~4: address nbytes bit3~0: dummy nbytes	21h	21h
852	SDR 1_1_1 fast read	cmd	0Bh	0Bh
853		bit7~4: address nbytes bit3~0: dummy nbytes	21h	21h
854	SDR 1_1_2 read (x2)	cmd	3Bh	3Bh
855		bit7~4: address nbytes bit3~0: dummy nbytes	21h	21h
856	SDR 1_2_2 read (dual)	cmd	BBh	BBh
857		bit7~4: address nbytes bit3~0: dummy nbytes	21h	21h
858	SDR 1_1_4 read (x4)	cmd	6Bh	6Bh
859		bit7~4: address nbytes bit3~0: dummy nbytes	21h	21h
860	SDR 1_4_4 read (Quad)	cmd	EBh	EBh
861		bit7~4: address nbytes bit3~0: dummy nbytes	22h	22h
862	SDR 1_1_8 read (x8)	cmd	00h	00h
863		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
864	SDR 1_8_8 read (Octal)	cmd	00h	00h
865		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
866	SDR 1_1_1 read (continuous)	cmd	03h	03h
867		bit7~4: address nbytes bit3~0: dummy nbytes	03h	03h
868	SDR 1_1_1 fast read (continuous)	cmd	0Bh	0Bh
869		bit7~4: address nbytes bit3~0: dummy nbytes	04h	04h
870	SDR 1_1_2 read (x2) (continuous)	cmd	3Bh	3Bh
871		bit7~4: address nbytes bit3~0: dummy nbytes	04h	04h
872	SDR 1_2_2 read (dual) (continuous)	cmd	BBh	BBh
873		bit7~4: address nbytes bit3~0: dummy nbytes	04h	04h
874	SDR 1_1_4 read (x4) (continuous)	cmd	6Bh	6Bh
875		bit7~4: address nbytes bit3~0: dummy nbytes	04h	04h
876	SDR 1_4_4 read (Quad) (continuous)	cmd	EBh	EBh
877		bit7~4: address nbytes bit3~0: dummy nbytes	06h	06h
878		cmd	00h	00h

879	SDR 1_1_8 read (x8) (continuous)	bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
880	SDR 1_8_8 read (Octal) (continuous)	cmd	00h	00h
881		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
882	DDR read ability- Continuous read bit7: 1_8_8 continuous read (0: no, 1: yes) bit6: 1_1_8 continuous read (0: no, 1: yes) bit5: 1_4_4 continuous read (0: no, 1: yes) bit4: 1_1_4 continuous read (0: no, 1: yes) bit3: 1_2_2 continuous read (0: no, 1: yes) bit2: 1_1_2 continuous read (0: no, 1: yes) bit1: 1_1_1 fast continuous read (0: no, 1: yes) bit0: 1_1_1 continuous read (0: no, 1: yes)		20h	20h
883	DDR read ability- Non-continuous read bit0: 1_1_1 (0: no, 1: yes) bit7: 1_8_8 (0: no, 1: yes) bit6: 1_1_8 (0: no, 1: yes) bit5: 1_4_4 (0: no, 1: yes) bit4: 1_1_4 (0: no, 1: yes) bit3: 1_2_2 (0: no, 1: yes) bit2: 1_1_2 (0: no, 1: yes) bit1: 1_1_1 (0: no, 1: yes) bit0: 1_1_1 (0: no, 1: yes)		20h	20h
884	DDR 1_1_1 read	cmd	00h	00h
885		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
886	DDR 1_1_1 fast read	cmd	00h	00h
887		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
888	DDR 1_1_2 read (x2)	cmd	00h	00h
889		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
890	DDR 1_2_2 read (dual)	cmd	00h	00h
891		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
892	DDR 1_1_4 read (x4)	cmd	00h	00h
893		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
894	DDR 1_4_4 read (quad)	cmd	EEh	EEh
895		bit7~4: address nbytes bit3~0: dummy nbytes	48h	48h
896	DDR 1_1_8 read (x8)	cmd	00h	00h

897		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
898	DDR 1_8_8 read (octal)	cmd	00h	00h
899		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
900	DDR 1_1_1 read (continuous)	cmd	00h	00h
901		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
902	DDR 1_1_1 fast read (continuous)	cmd	00h	00h
903		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
904	DDR 1_1_2 read (x2) (continuous)	cmd	00h	00h
905		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
906	DDR 1_2_2 read (dual) (continuous)	cmd	00h	00h
907		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
908	DDR 1_1_4 read (x4) (continuous)	cmd	00h	00h
909		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
910	DDR 1_4_4 read (quad) (continuous)	cmd	EEh	EEh
911		bit7~4: address nbytes bit3~0: dummy nbytes	0Ch	0Ch
912	DDR 1_1_8 read (x8) (continuous)	cmd	00h	00h
913		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
914	DDR 1_8_8 read (octal) (continuous)	cmd	00h	00h
915		bit7~4: address nbytes bit3~0: dummy nbytes	00h	00h
916	SDR write ability (Progam load) bit7~2: reserved bit1: 1_1_4 write (0: no, 1: yes) bit0: 1_1_1 write (0: no, 1: yes)		03h	03h
917	SDR 1_1_1 write	cmd	02h	02h
918		bit7~4: address nbytes bit3~0: dummy nbytes	20h	20h
919	SDR 1_1_4 write (x4)	cmd	32h	32h
920		bit7~4: address nbytes bit3~0: dummy nbytes	20h	20h

921-932	reserved		00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h	00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h
933	DDR write ability (reserved) bit7~0: reserved		00h	00h
934-949	reserved		00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h	00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h
950	SDR update ability (Program Load Random Data) bit7~2: reserved bit1: 1_1_4 update (0: no, 1: yes) bit0: 1_1_1 update (0: no, 1: yes)		03h	03h
951	SDR 1_1_1 update	cmd	84h	84h
952		bit7~4: address nbytes bit3~0: dummy nbytes	20h	20h
953	SDR 1_1_4 update	cmd	34h	34h
954		bit7~4: address nbytes bit3~0: dummy nbytes	20h	20h

955-966	reserved		00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h	00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h
967	DDR update ability (Reserved) bit7~0: reserved		00h	00h
968-983	reserved		00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h	00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h 00h
984	OOB overall layout	0: Discrete 1: Continuous	01h	01h
985	OOB free layout	OOB free start	00h	00h
986		OOB free length	10h	10h
987		BBM (bad block mark) length	02h	02h
988	ECC parity layout	ECC parity start	40h	40h
989		ECC parity space	10h	10h
990		ECC parity (real) length	10h	10h
991	Advanced ECC status CMD0 (higher bit)	cmd value	0Fh	0Fh
992		addr val	C0h	C0h
993		addr nbytes	01h	01h
994		addr buswidth	01h	01h
995		dummy nbytes	00h	00h
996		dummy buswidth	00h	00h

997		status bytes (max=2)	01h	01h
998		status register mask0	00h	00h
999		status register mask1	30h	30h
1000		post process operator: 0: none 1: & 2: +	00h	00h
1001		post process mask	00h	00h
1002	Advanced ECC status CMD1 (lower bit)	cmd value	0Fh	0Fh
1003		addr val	F0h	F0h
1004		addr nbytes	01h	01h
1005		addr buswidth	01h	01h
1006		dummy nbytes	00h	00h
1007		dummy buswidth	00h	00h
1008		status bytes (max=2)	01h	01h
1009		status register mask0	00h	00h
1010		status register mask1	30h	30h
1011		post process operator: 0: none 1: & 2: +	00h	00h
1012		post process mask	00h	00h
1013	ECC no error status		00h	00h
1014	ECC uncorrectable status		08h	08h
1015	If correctable bitflips happen (return ECC max if number exceeds ECC max capability)	post process operator: 0: none 1: & 2: + 3: -	00h	00h
1016		post process mask	00h	00h
1017-1021	Reserved		00h 00h 00h 00h 00h	00h 00h 00h 00h 00h
1022-1023	Integrity CRC			
1024-1279	Value of bytes 768-1023		Same as 768-1023Byte	Same as 768-1023Byte
1280-1535	Value of bytes 768-1023		Same as 768-1023Byte	Same as 768-1023Byte

Notes:

1. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the CASN page were transferred correctly to the host. The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X^{16} + X^{15} + X^2 + 1$, This polynomial in hex may be represented as 8005h.
2. The CRC value shall be initialized with a value of 4341h before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Device Model	ORGANIZATION	VCC RANGE	CRC value B1022/B1023
“GD5F1GM9UE”	X4	2.7v ~ 3.6v	51h/28h
“GD5F1GM9RE”	X4	1.7v ~ 2.0v	A9h/3Fh

11 PROGRAM OPERATIONS

11.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to whole page bytes of data within a page. The page program sequence is as follows:

- 02h (PROGRAM LOAD)/32h (PROGRAM LOAD x4)
- 06h (WRITE ENABLE)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Firstly, a PROGRAM LOAD (02h/32h) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The Program address should be in sequential order in a block. The data bytes are loaded into a cache register that is whole page long. If more than one page data are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure11-1 shows the PROGRAM LOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

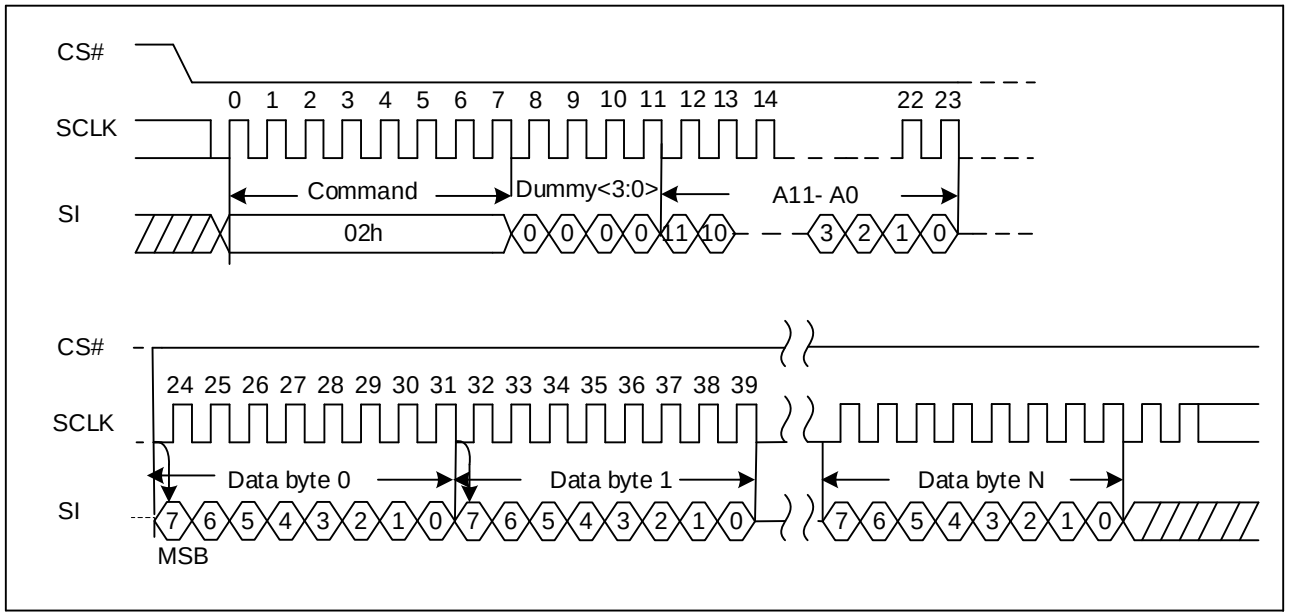
Note:

1. The contents of Cache Register don’t reset when Program Random Load (84h/C4h/34h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h/32h) command, the 0xFF is output to the address that data was not loaded by Program Load (02h/32h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h/C4h/34h) command, the contents of Cache Register are output to the NAND.
4. The Program address should be in sequential order in a block.
5. Program Load x4 is only available with the QE enable.

11.2 Program Load (PL) (02h)

The command sequence is shown below.

Figure 11-1. Program Load Sequence Diagram

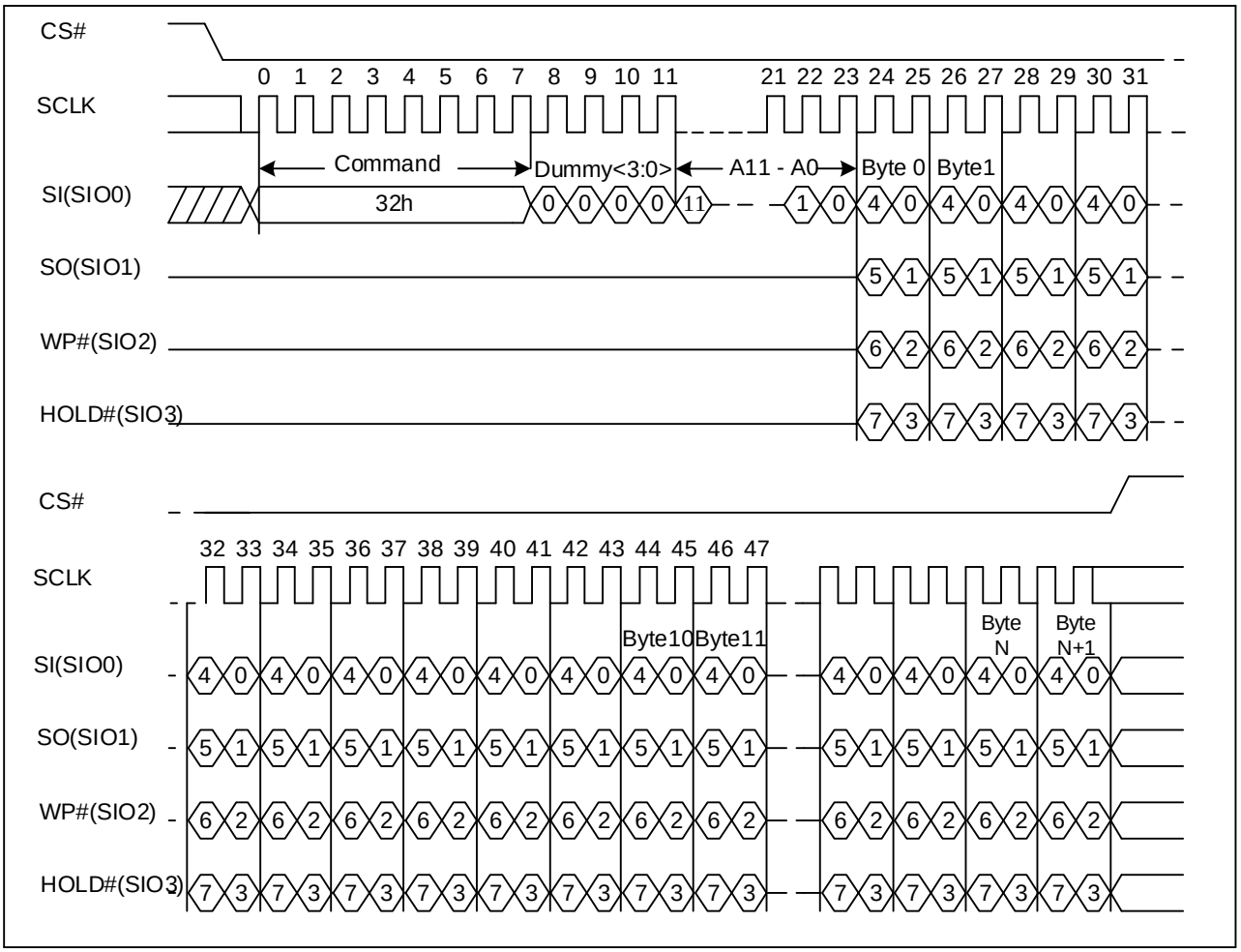


Note: When internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

11.3 Program Load x4 (PL x4) (32h)

The Program Load x4 command (32h) is similar to the Program Load command (02h) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command.

Figure 11-2. Program Load x4 Sequence Diagram

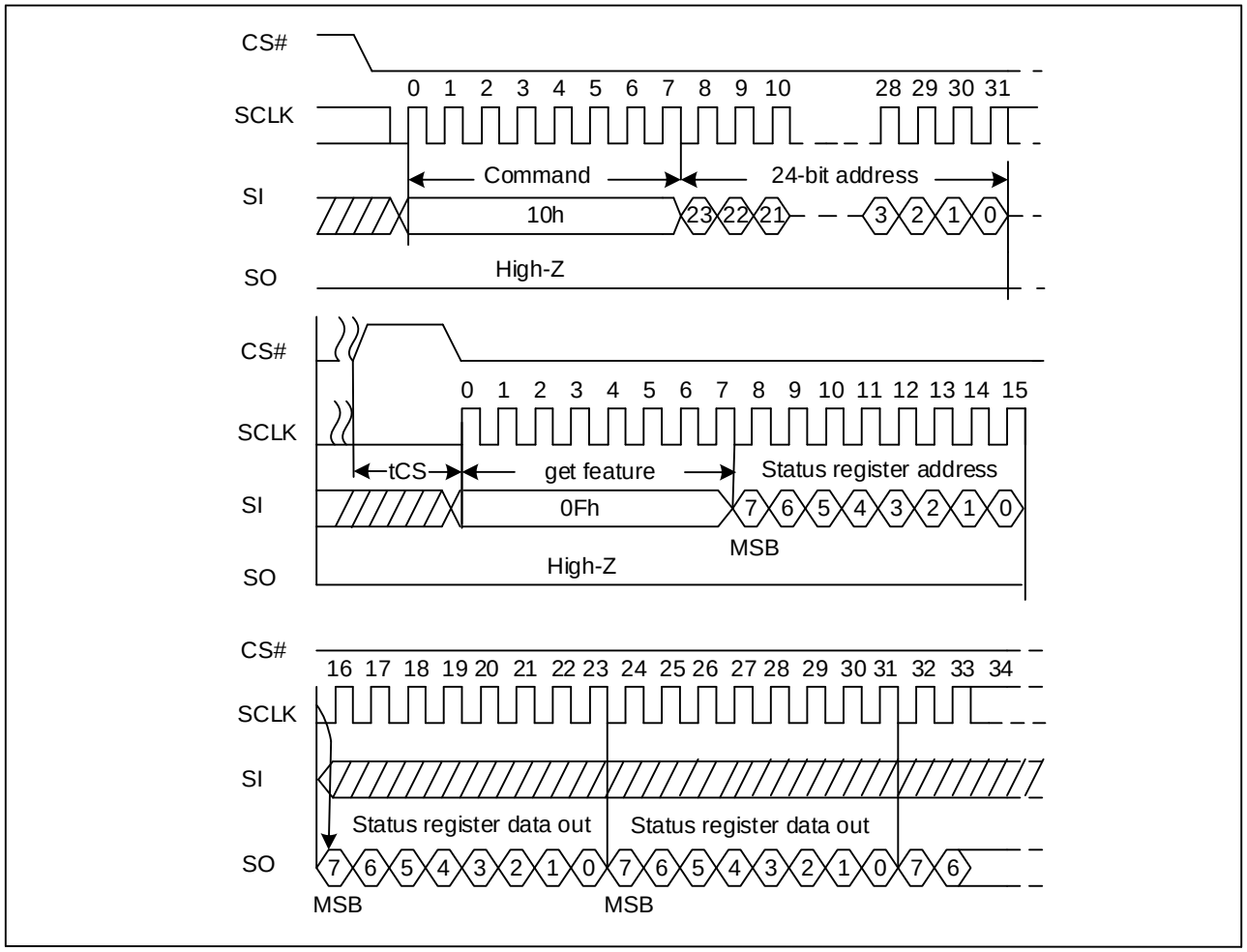


Note: When internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

11.4 Program Execute (PE) (10h)

After the data is loaded, a PROGRAM EXECUTE (10h) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation shown in Figure11-3. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command. The command sequence is shown below.

Figure 11-3. Program Execute Sequence Diagram



11.5 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

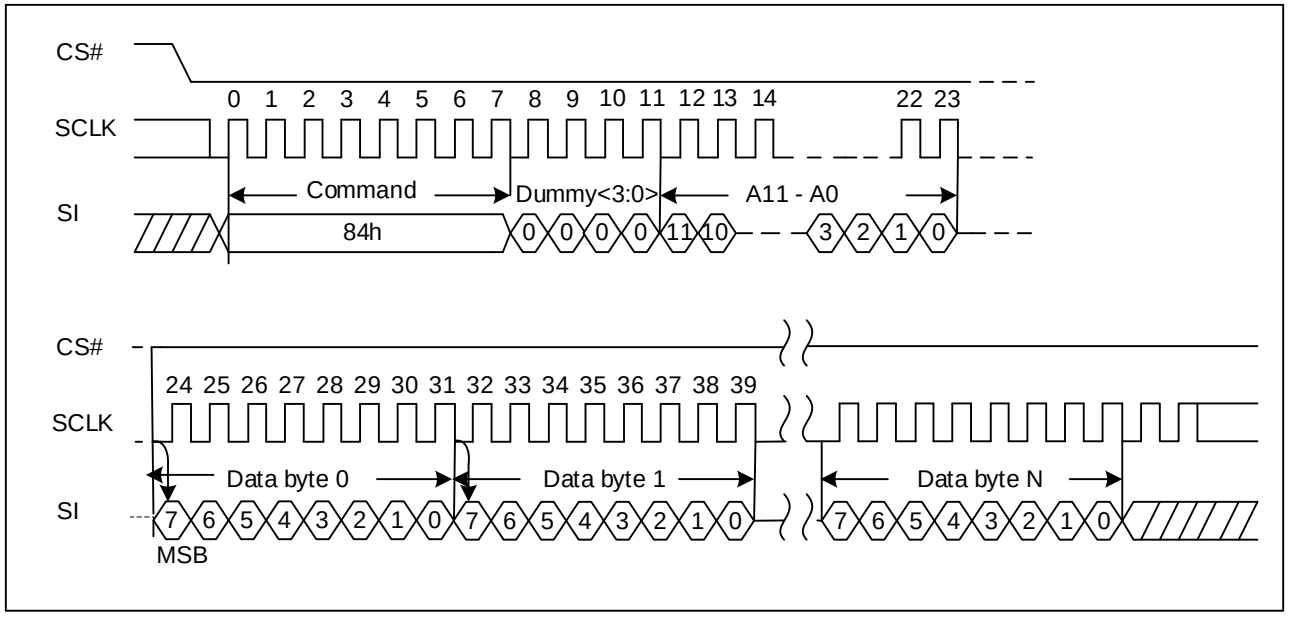
- 13h (PAGE READ to cache)
- Optional 84h/C4h/34h (PROGRAM LOAD RANDOM DATA)
- 06h (WRITE ENABLE)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13h) command. The PROGRAM LOAD RANDOM DATA (84h/C4h) command can be issued, if user wants to update bytes of data in the page. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h/C4h) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then PROGRAMEXECUTE (10h) command can be issued to start the programming operation.

11.6 Program Load Random Data (84h)

This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h) command must be issued with a new column address, see figure11-4 for details. This command is only available during internal data moves sequence.

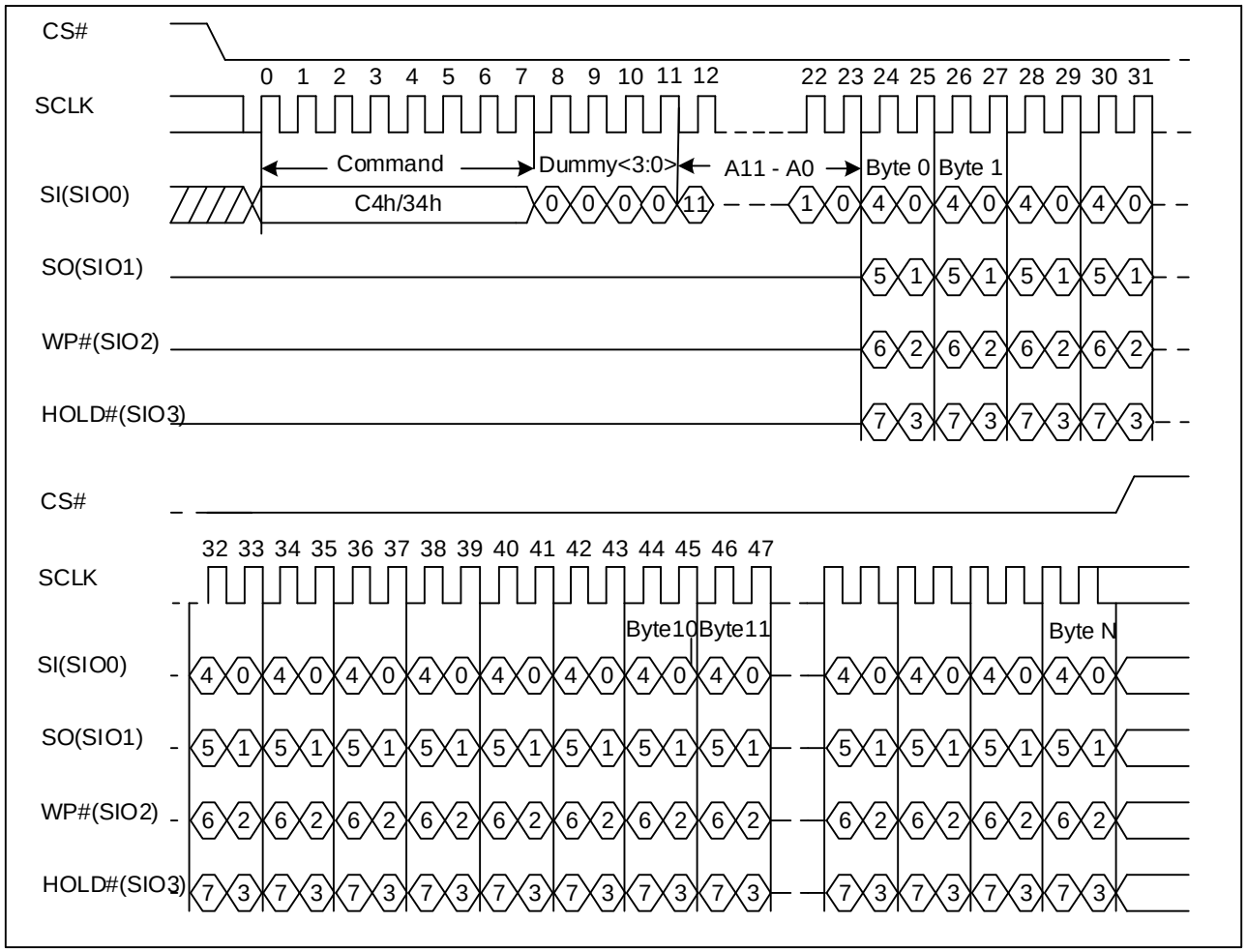
Figure 11-4. Program Load Random Data Sequence Diagram



11.7 Program Load Random Data x4 (C4h/34h)

The Program Load Random Data x4 command (C4h/34h) is similar to the Program Load Random Data command (84h) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command. See Figure11-5 for details. Those two commands are only available during internal data move sequence.

Figure 11-5. Program Load Random Data x4 Sequence Diagram



12 ERASE OPERATIONS

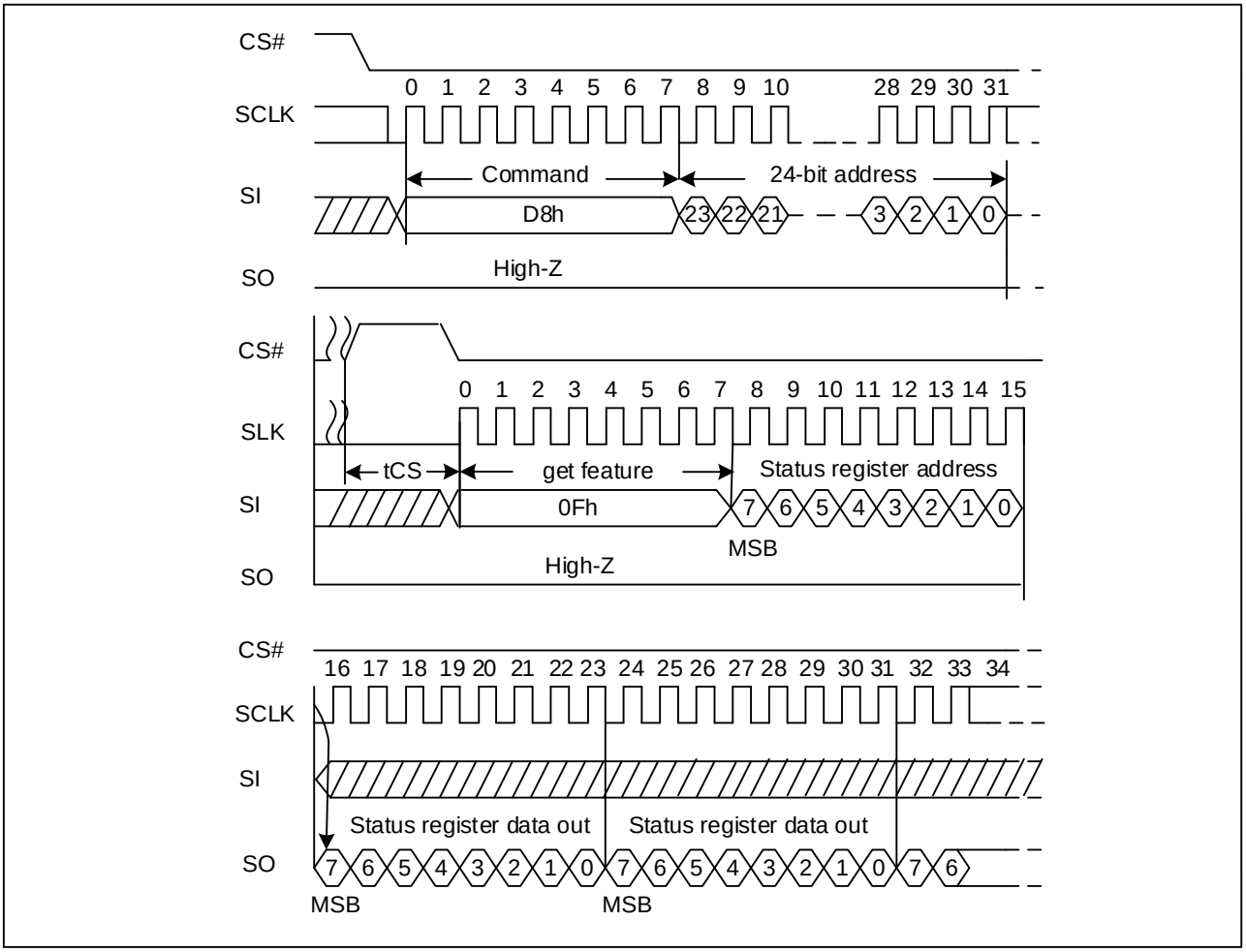
12.1 Block Erase (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for t_{BERS} time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation.

Figure 12. Block Erase Sequence Diagram

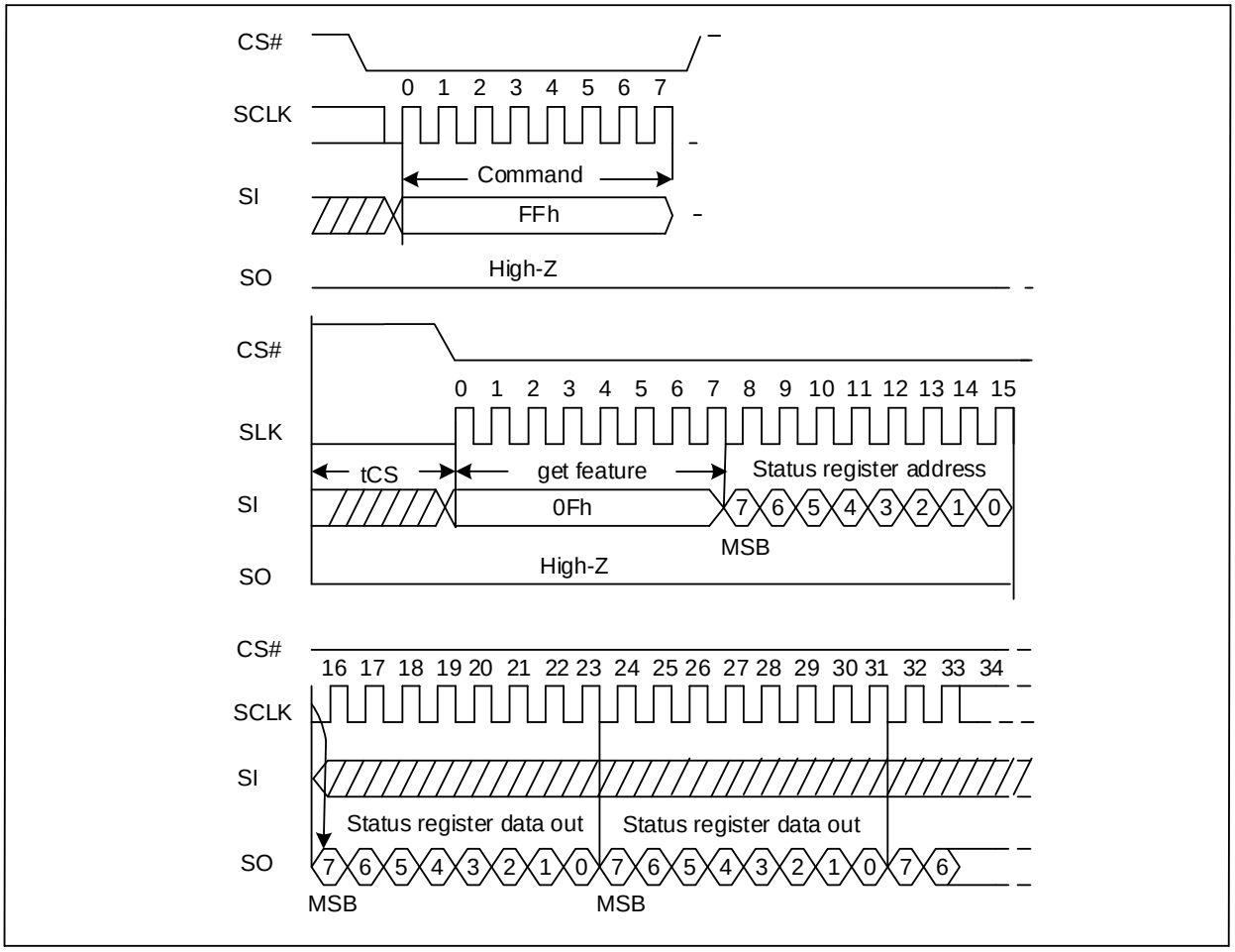


13 RESET OPERATIONS

13.1 Soft Reset (FFh)

The RESET (FFh) command stops all operations and the status. For example, in case of a program or erase or read operation, the reset command can make the device enter the idle state.

Figure 13-1. Reset Sequence Diagram



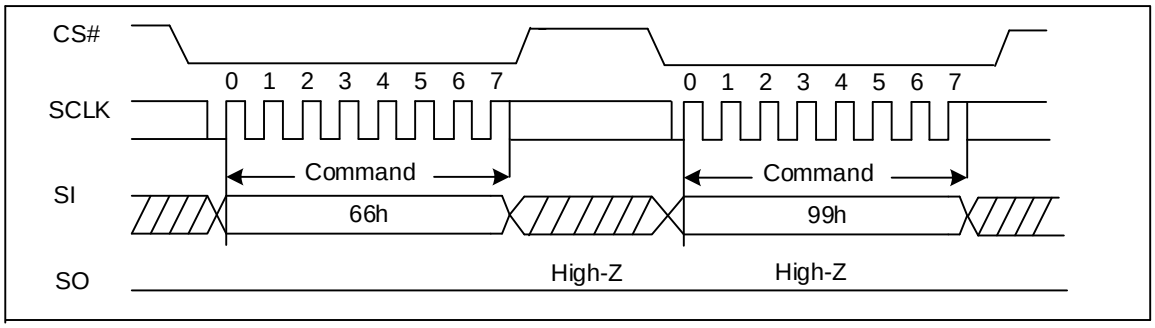
Note: The Register bit value after soft reset refers to Table 6. Register bit Descriptions.

13.2 Enable Power on Reset (66h) and Power on Reset (99h)

If the Power on Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current feature settings.

The “Enable Reset (66h)” and the “Reset (99h)” commands can be issued in SPI mode. The “Reset (99h)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tVSL to reset. During this period, no command will be accepted. It is recommended to check the OIP bit in Status Register before issuing any other command sequence.

Figure 13-2. Reset Sequence Diagram



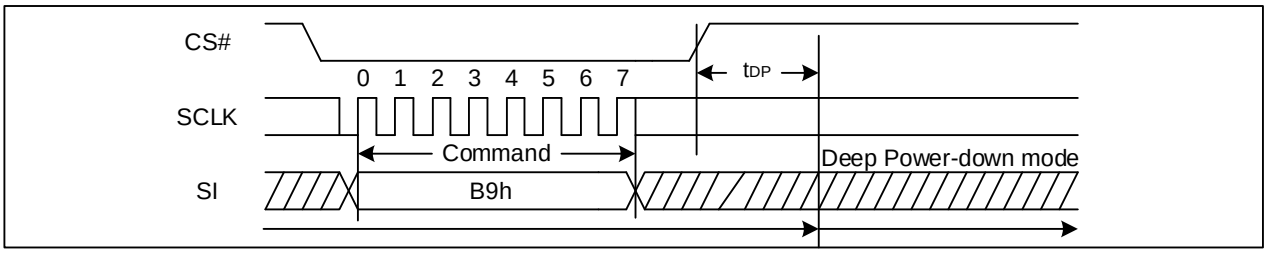
14 Deep Power-Down Mode (1.8V Only)

14.1 Enter Deep Power-Down (B9h)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down (ABh), Soft Reset (FFh) or Enable Reset (66h) and Reset (99h) commands. These commands can release the device from this mode. The Release from Deep Power-Down command releases the device from deep power down mode.

The Deep Power-Down Mode automatically stops at Power-Down, and the device is in the Standby Mode after Power-Up. The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC1} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 14-1 Deep Power-Down Sequence Diagram

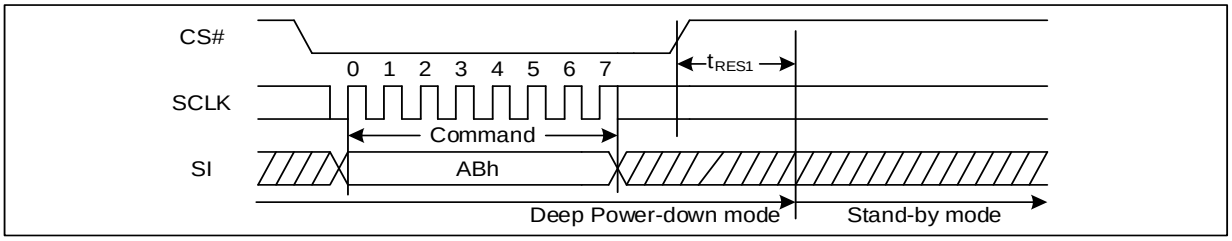


14.2 Release from Deep Power-Down (ABh)

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used to release the device from the Power-Down state, the command is the same as previously described, After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down command is issued while an Erase, Program or Write cycle is in process (when OIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 14-2. Release Power-Down Sequence Diagram



Note：

(1) FFh/ABh can get off from the DPD. About tRES1, user can get feature to check OIP if it’s ready.

(2) 66h+99h will terminate the DPD. About tVSL the device will return to its default power-on state and lose all the current feature settings.

15 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (NVB) of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

To simplify the system requirement and guard the data integration, GigaDevice SPI NAND provides assistant Management options as below.

Table 15-1. Bad Block Mark information (1Gb)

Description	Requirement
Minimum number of valid blocks (NVB)	1004
Total available blocks per die	1024
First spare area location	Byte 2048
Bad-block mark	00h (use non FFh to check)

15.1 Bad Block Management (A1h)

The Product offers a convenient method to manage the bad blocks logical address. This function allows the user to replace the bad block with the good block that exist at the shipment and after extensive use to ensure that the logical block address is available and continuous.

The Bad Block Management(A1h) command consists of 6-bit dummy&10-bit Logical Block Address(LBA) and 6-bit dummy&10-bit Physical Block Address(PBA). The Write Enable(06h) command must be executed before the device will accept the Bad Block Management command. The original bad block will be replaced by the selected good block, and the original bad block logical address will be available. After that, the selected good block logical address will be unavailable.

Once a Bad Block Management command is successfully executed, there will be a bad block link added to the Bad Block Link Table. The product can provide 20 links in Bad Block Link Table. If all 20 links have been used, the BBLS (Bad Block Link Status) will change to 1. And no more bad block links can be used to replace the bad block. Therefore, it's recommended to check the BBLS bit or issue the Read Bad Block Link Table command to confirm if any spare links are still available.

The manufacturer may have used some of the bad block links to guarantee the continuous good blocks at the shipment.

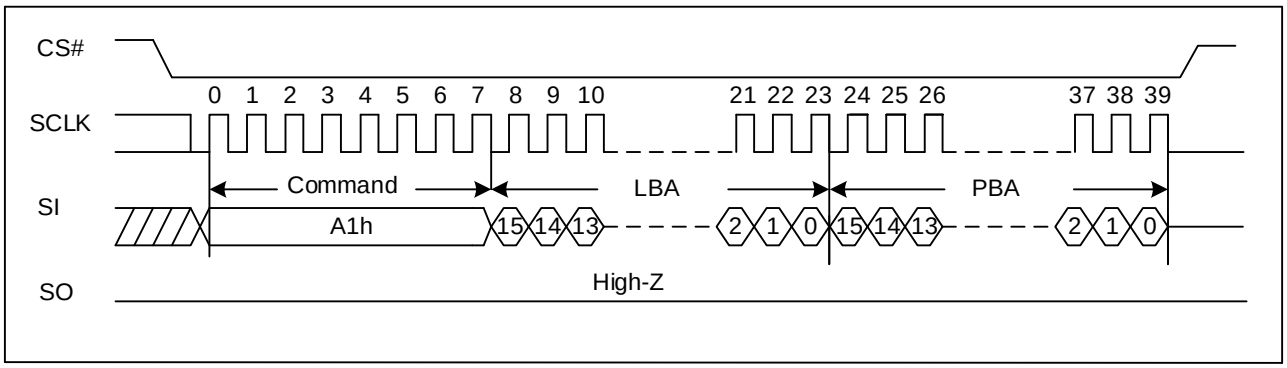
- Issus the Write Enable (06h) command (WEL=1)
- Issue the Write Bad Block Management (A1h) command. Wait for tPROG time.

Note:

1. The same address in multiple PBAS (physical) is prohibited.

2.Since the initial bad block mark is stored in the PBA, that the LBA linked to different PBA may cause the initial bad block mark to be unrecognized. We recommend that the user create their own Bad Block Table with LBA by reading all of the block during the first use after shipment.

Figure 15-1. Bad Block Management



15.2 Read Bad Block Link Table (A5h)

The Bad Block Link Table consists 20 LBA-PBA links (from LBA0-PBA0 to LBA19-PBA19). The Read Bad Block Link Table command can be used to check the existing address links stored inside the table.

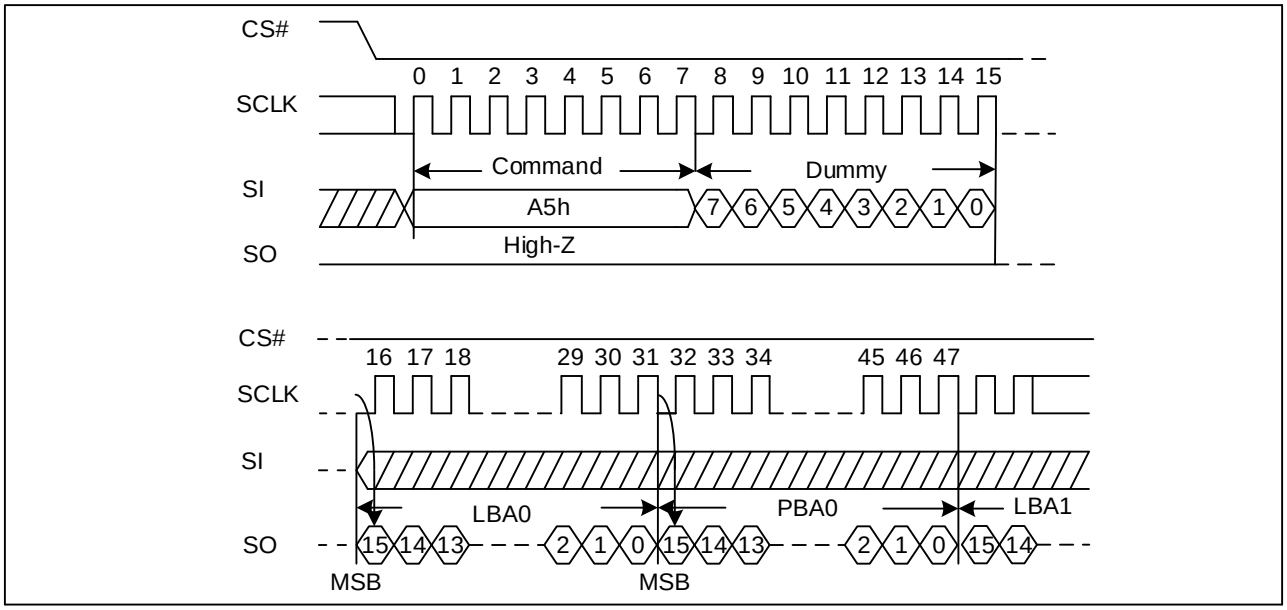
The Read Bad Block Link Table(A5h) command consist of 8-bit Dummy Clocks. Then the device will start to output the 6-bit dummy&10-bit Logical Block Address (LBA) and the 6-bit dummy&10-bit Physical Block Address (PBA). All block address links will be output sequentially starting from the first link (LBA0-PBA0) to the end link (LBA19-PBA19). If there are available links, the output will contain all “00h” data.

The MSB bits LBA [15:14] of each link are used to indicate the status of the link.

Table 15-2. LBA [15:14] Description

LBA [15]	LBA [14]	Description
0	0	This link is available to use
1	0	This link has been used and it is a valid link.
1	1	This link has been used and it is not valid.
0	1	NA

Figure 15-2. Read Bad Block Link Table

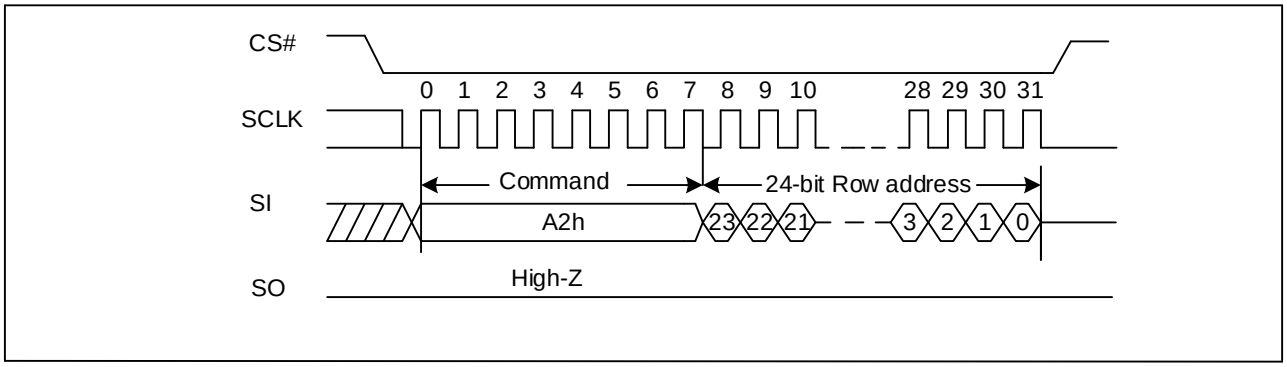


16 Write power-on Page Address (A2h)

The device will automatically read first page of first block to cache after power on, then host can directly read data from cache for easy boot. This command allows the user to change the power-on page address. The power-on page address is OTP address. Once new the power-on page address is accepted, it will be permanently locked that can't be changed. And the new page will be auto load to cache register from next power-on.

- Issus the Write Enable (06h) command (WEL=1)
- Issue the Write power-on Page Address (A2h) command. Wait for tPROG time

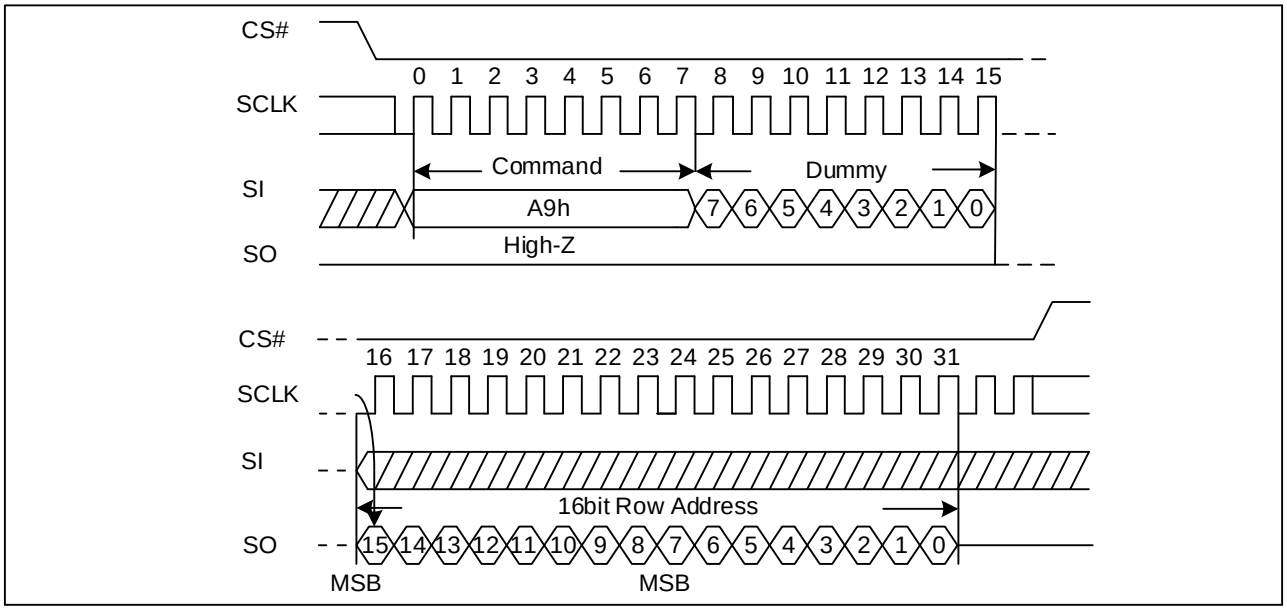
Figure 16. Write power-on Page Address



17 Read ECC Warning Page Address (A9h)

The user can get the last page address which reaches the Internal ECC warning setting in the continuous read mode. The ECC bit Flip Threshold Register (10h) can set the ECC warning standard by the users. FFh command doesn't clear the ECC Warning Page Address.

Figure 17. Read ECC Warning Page Address



BFT3	BFT2	BFT1	BFT0	
0	0	0	0	Detect the uncorrectable error
0	0	0	1	Detect the uncorrectable error
0	0	1	0	Detect the uncorrectable error
0	0	1	1	Detect the uncorrectable error
0	1	0	0	Detect the uncorrectable error
0	1	0	1	Detect 5 bit flip in a sector
0	1	1	0	Detect 6 bit flip in a sector
0	1	1	1	Detect 7 bit flip in a sector
1	0	0	0	Detect 8 bit flip in a sector
1	0	0	1	Detect the uncorrectable error
1	0	1	0	Detect the uncorrectable error
1	0	1	1	Detect the uncorrectable error
1	1	0	0	Detect the uncorrectable error
1	1	0	1	Detect the uncorrectable error
1	1	1	0	Detect the uncorrectable error
1	1	1	1	Detect the uncorrectable error (Default)

18 Read ECC Status Command (7Ch)

The Read ECC Status Command (7Ch) are used to monitor the device Internal ECC status after the read operation.

The output data of the command is the same as the 4bit ECC Status (ECCS1, ECCS0, ECCSE1, ECCSE0) in the Feature Register. The purpose of this command is to provide the user with a quick way to read ECC Status instead of the complex get feature method.

This command is only available with Internal ECC on.

Figure 18. Read ECC Status Command Sequence

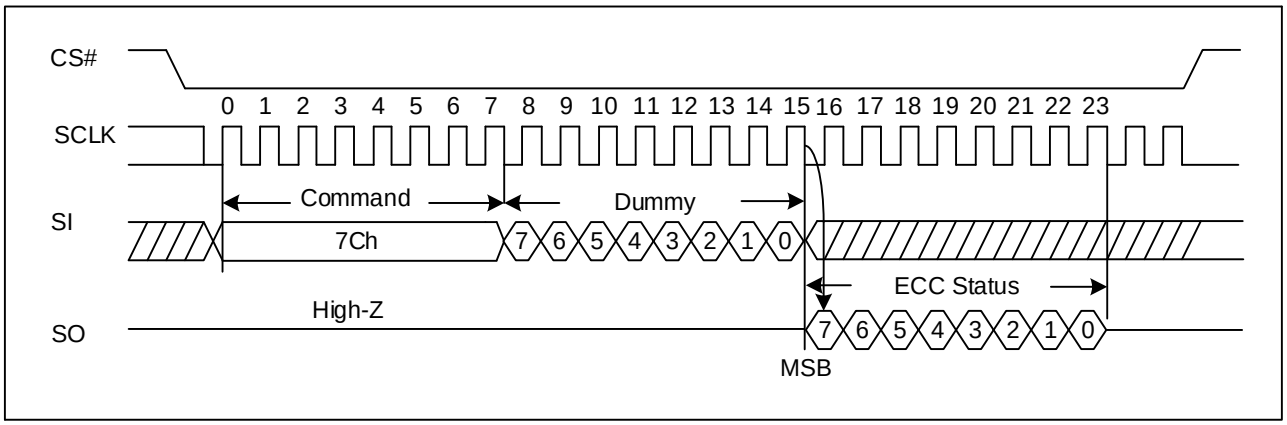


Table 18. ECC Status Output Structure

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Internal ECC Status for the accumulated pages				Internal ECC status for the current page			
ECCS1	ECCS0	ECCSE1	ECCSE0	ECCS1	ECCS0	ECCSE1	ECCSE0

Note: ECC Status for the accumulated pages is only in continuous read mode. In normal read, bit7~bit4 will indicate the current page internal ECC status.

ECCS1	ECCS0	ECCSE1	ECCSE0	Description
0	0	x	X	No bit errors were detected during the previous read algorithm
0	1	0	0	Bit errors (≤4) were detected and corrected
0	1	0	1	Bit errors (=5) were detected and corrected.
0	1	1	0	Bit errors (=6) were detected and corrected.
0	1	1	1	Bit errors (=7) were detected and corrected.
1	1	x	X	Bit errors (=8) were detected and corrected.
1	0	x	X	Bit errors greater than ECC capability (8 bits) and not corrected

19 POWER ON TIMING

Figure 19. Power on Timing Sequence

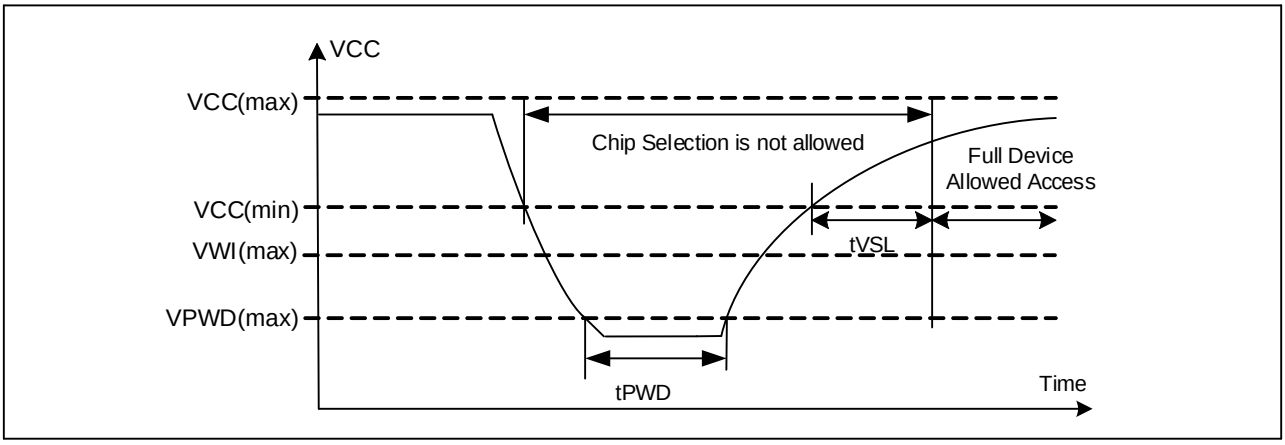


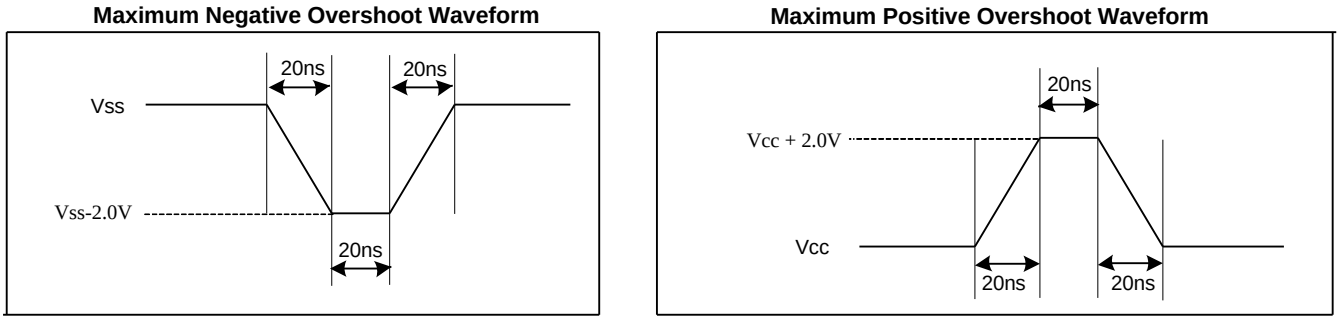
Table 19. Power-On Timing and Write Inhibit Threshold for 1.8V/3.3V

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	2		ms
VWI	Write Inhibit Voltage (1.8V)		1.5	V
VWI	Write Inhibit Voltage (3.3V)		2.5	V
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	50		µs

20 ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85 / -40 to 105	℃
Storage Temperature	-65 to 150	℃
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
VCC (3.3V)	-0.6 to 4.0	V
VCC (1.8V)	-0.6 to 2.5	V

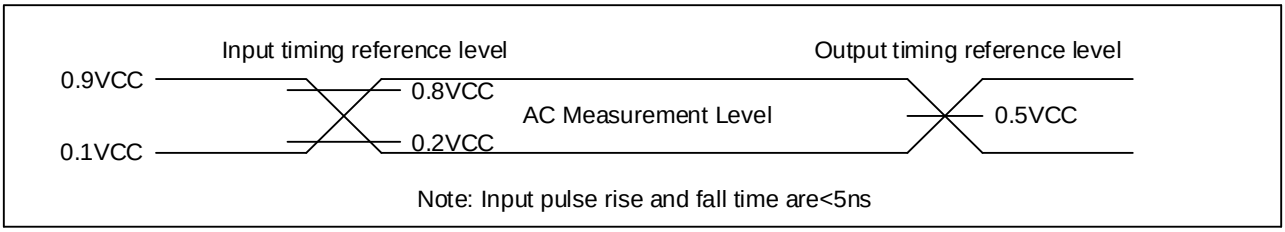
Figure 20. Input Test Waveform and Measurement Level



21 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.9VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.8VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 21. Input Test Waveform and Measurement Level



22 DC CHARACTERISTIC

(T= -40℃~85℃/-40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±10	μA
I_{LO}	Output Leakage Current				±10	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		10	50	μA
I_{CC2}	Operating Current (Read) In Normal Read	CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open (*1, *2, *4 I/O)		15	30	mA
I_{CC2}	Operating Current (Read) In Continuous Read	CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open (*1, *2, *4 I/O)		35	50	mA
I_{CC2}	Operating Current (Read) In Continuous Read	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open (*1, *2, *4 I/O)		30	50	mA
I_{CC3}	Operating Current (Program)			15	30	mA
I_{CC4}	Operating Current (Erase)			15	30	mA
I_{CC5}	Operating Current (Read)			15	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note:

Value guaranteed by design and/or characterization, not 100% tested in production.

(T= -40℃~85℃/105℃, VCC=1.7~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±10	μA
I_{LO}	Output Leakage Current				±10	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		10	50	μA
$I_{CC1-DPD}$	Standby Current Deep Power Down Mode (1.8V only)			1	5	uA
I_{CC2}	Operating Current (Read) In Normal Read	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open (*1, *2, *4 I/O)		10	30	mA
I_{CC2}	Operating Current (Read) In Continuous Read	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open (*1, *2, *4 I/O)		25	35	mA
I_{CC3}	Operating Current (Program)			10	30	mA
I_{CC4}	Operating Current (Erase)			10	30	mA
I_{CC5}	Operating Current (Read)			10	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

23 AC CHARACTERISTICS

(T= -40℃~85℃, VCC=1.7~2.0V/2.7~3.6V, C_L=30pf)

Symbol	Parameter	1.8V		3.3V		Unit.
		Min.	Max.	Min.	Max.	
FC(1)	Serial Clock Frequency		133(1)		166(1)	MHz
FC_DTR	Serial Clock Frequency of DTR		104		133	MHz
tCH	Serial Clock High Time	3.375		2.7		ns
tCL	Serial Clock Low Time	3.375		2.7		ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2		0.1		V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2		0.1		V/ns
tCHSH	CS# Active Hold Time	5		5		ns
tSHCH	CS# Not Active Setup Time	5		5		ns
tSLCH	CS# Active Setup Time	5		5		ns
tCHSL	CS# Not Active Hold Time	5		5		ns
tSHSL/tCS	CS# High Time	20		15		ns
tSHQZ	Output Disable Time		20		10	ns
tCLQX	Output Hold Time	1.5		1		ns
tCHQX	Output Hold Time (DTR Only)	1.5		1		ns
tDVCH	Data In Setup Time (STD&DTR)	2		2		ns
tCHDX	Data In Hold Time (STR&DTR)	2		2		ns
tDVCL	Data In Setup Time (DTR Only)	2		2		ns
tCLDX	Data In Hold Time (DTR Only)	2		2		ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5		4		ns
tHHCH	Hold# High Setup Time (relative to Clock)	5		4		ns
tCHHL	Hold# High Hold Time (relative to Clock)	2		2		ns
tCHHH	Hold# Low Hold Time (relative to Clock)	2		2		ns
tHLQZ	Hold# Low To High-Z Output		15		15	ns
tHHQX	Hold# High To Low-Z Output		15		10	ns
tCLQV	Clock Low To Output Valid (10pf)		7.5		6	ns
tCLQV	Clock Low To Output Valid (30pf)		9		7	ns
tCHQV	Clock High To Output Valid (DTR Only) (10pf)		7.5		6	ns
tCHQV	Clock High To Output Valid (DTR Only) (30pf)		9		7	
tWHSL	WP# Setup Time Before CS# Low	20		20		ns
tSHWL	WP# Hold Time After CS# High	100		100		ns
tDP	CS# High To Deep Power-Down Mode		3		--	μs
tRES1	CS# High To Standby Mode		50		--	μs
tQSV	Clock transient to DQS valid time	Align to 30pF tCLQV				ns
tDQSQ	SIO Valid Skew Related to DQS (TFBGA24/SOP16, 12pF)		0.7		0.7	ns
tQHS	SIO Hold Skew Factor (TFBGA24/SOP16, 12pF)		0.7		0.7	ns

Note:

(1) Please refer to the frequency table7-5 Read from Cache command in different read mode.

(2) Value guaranteed by design and/or characterization, not 100% tested in production

24 PERFORMANCE AND TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRST	CS# High To Next Command After Reset (FFh) Read/Program/Erase			5/10/500	us
tRD	Read From Array			25	us
tRD_ECC	Read From Array with ECC		50	150	us
Fast RD_ECC	Read From Array with ECC (AL=1)		30	80	us
tCBSYR	Cache busy time for Cache Read		5	25	us
tCBSYR_ECC	Cache busy time for Cache Read with ECC		30	80	Us
tPROG	Page Programming Time		300	600	us
tPROG_ECC	Page Programming Time with ECC		320	600	us
tBERS	Block Erase Time		3	10	ms

Figure 24-1. Serial Input Timing

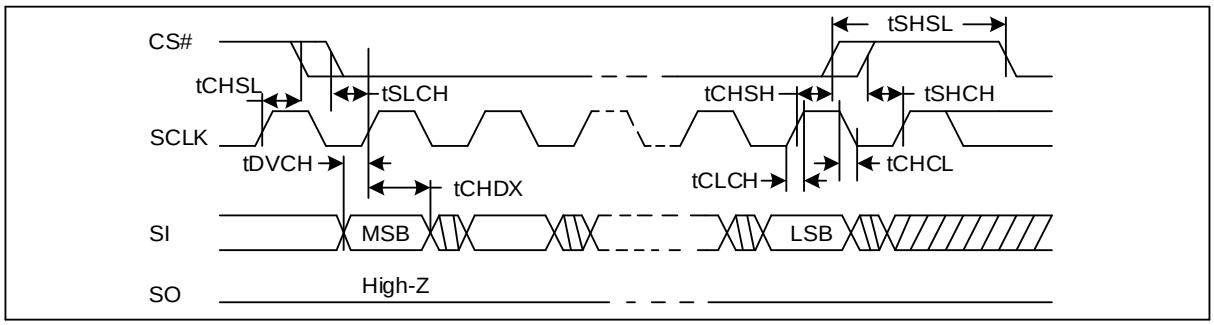


Figure 24-2. Output Timing

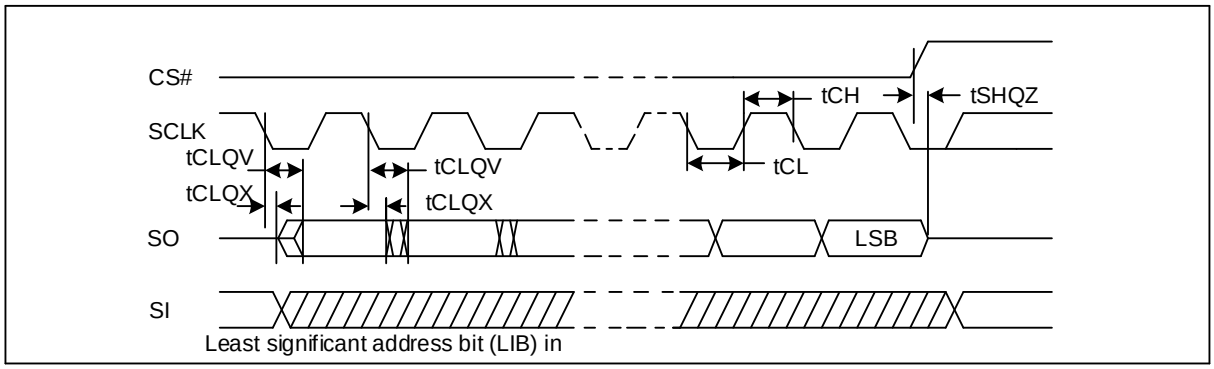


Figure 24-3. Serial Input Timing (DTR)

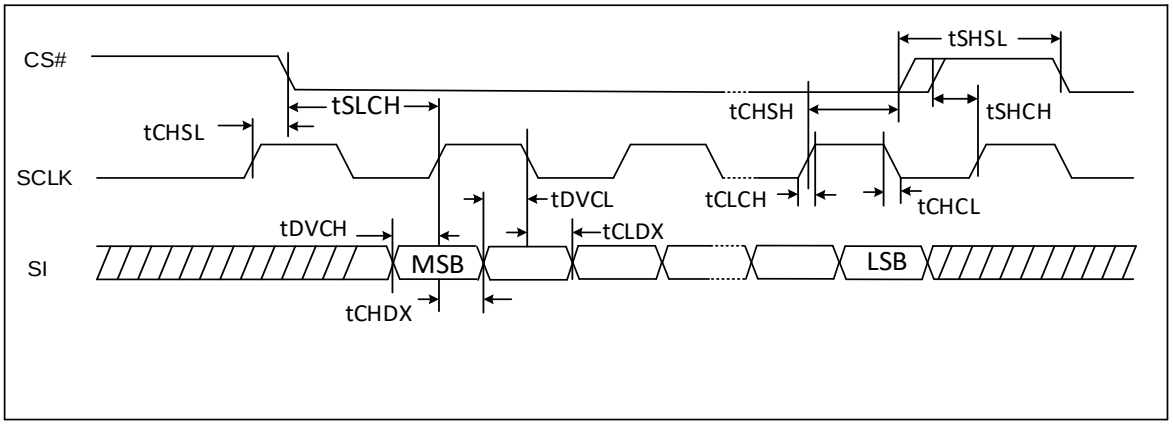


Figure 24-4. Serial Output Timing (DTR)

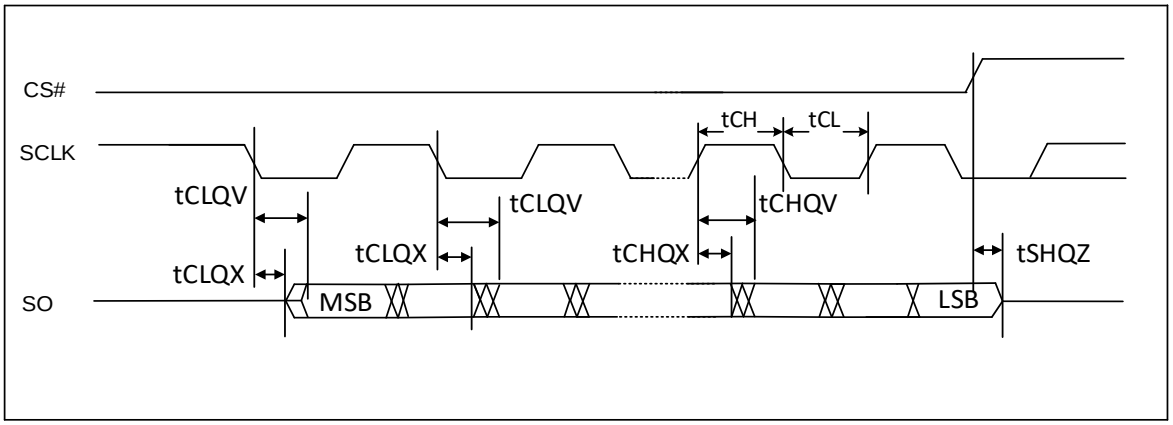


Figure 24-5. Serial Output Timing (DTR with DQS)

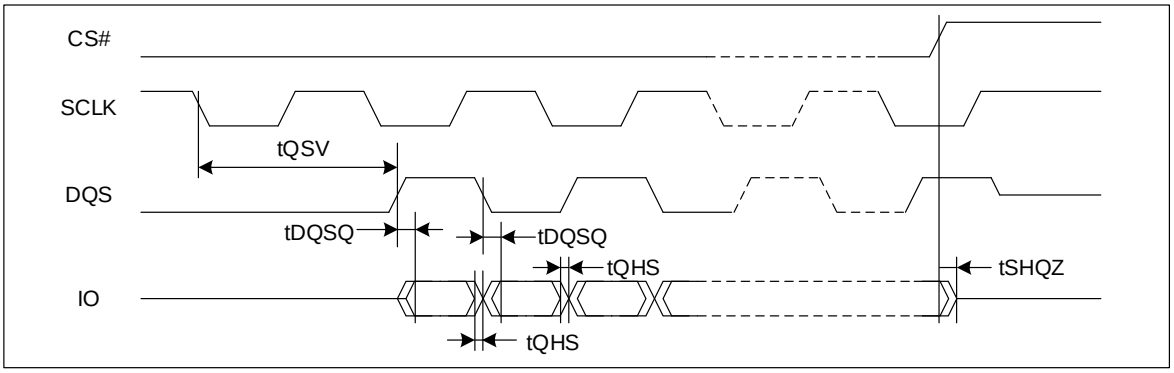


Figure 24-6. Hold# Timing

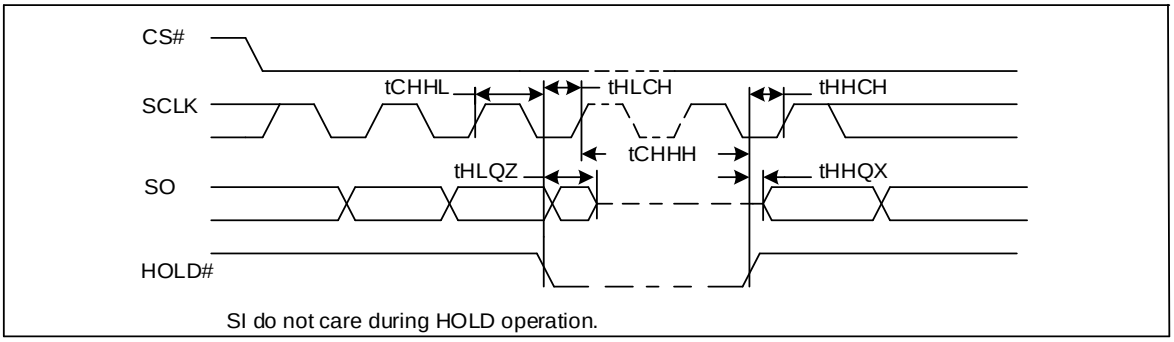
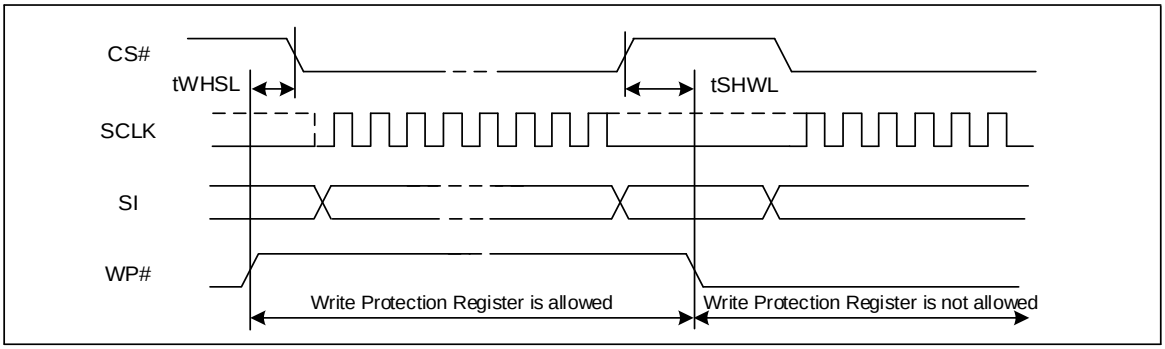
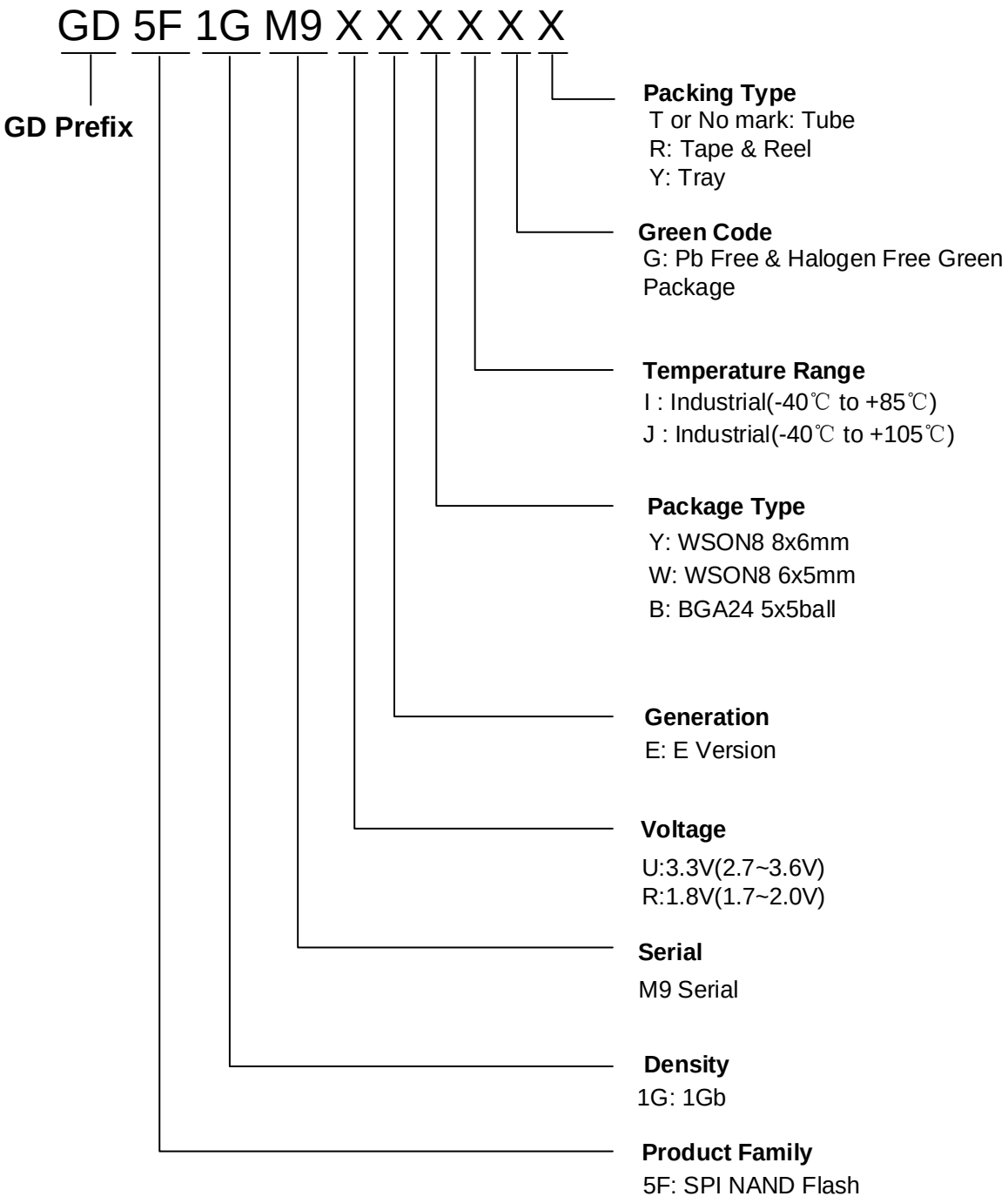


Figure 24-7. WP# Timing

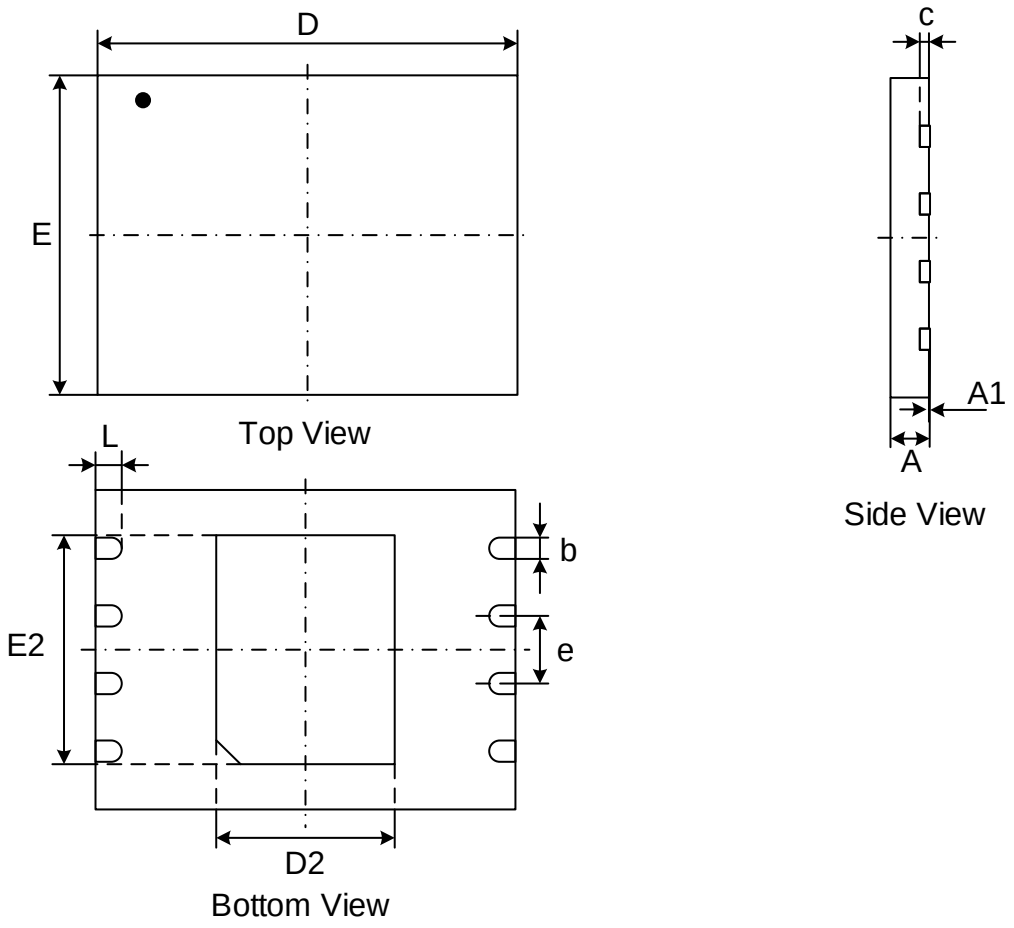


25 ORDERING INFORMATION



26 PACKAGE INFORMATION

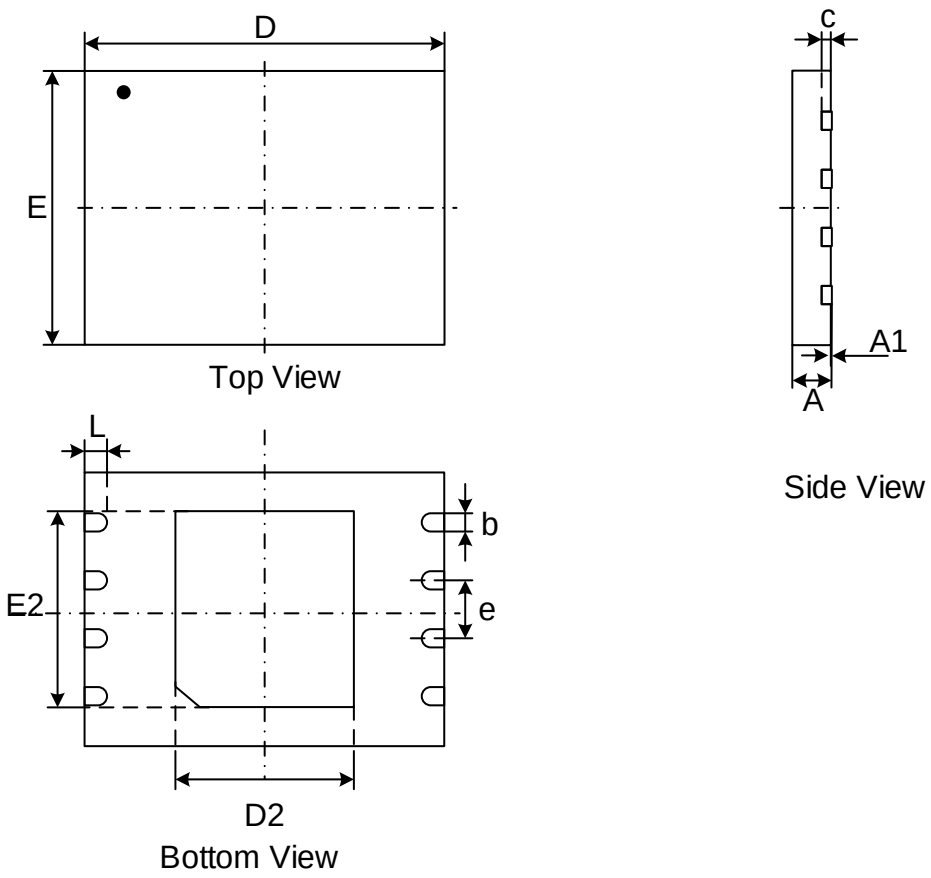
Figure 26-1. WSON8 (8*6mm)



Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022

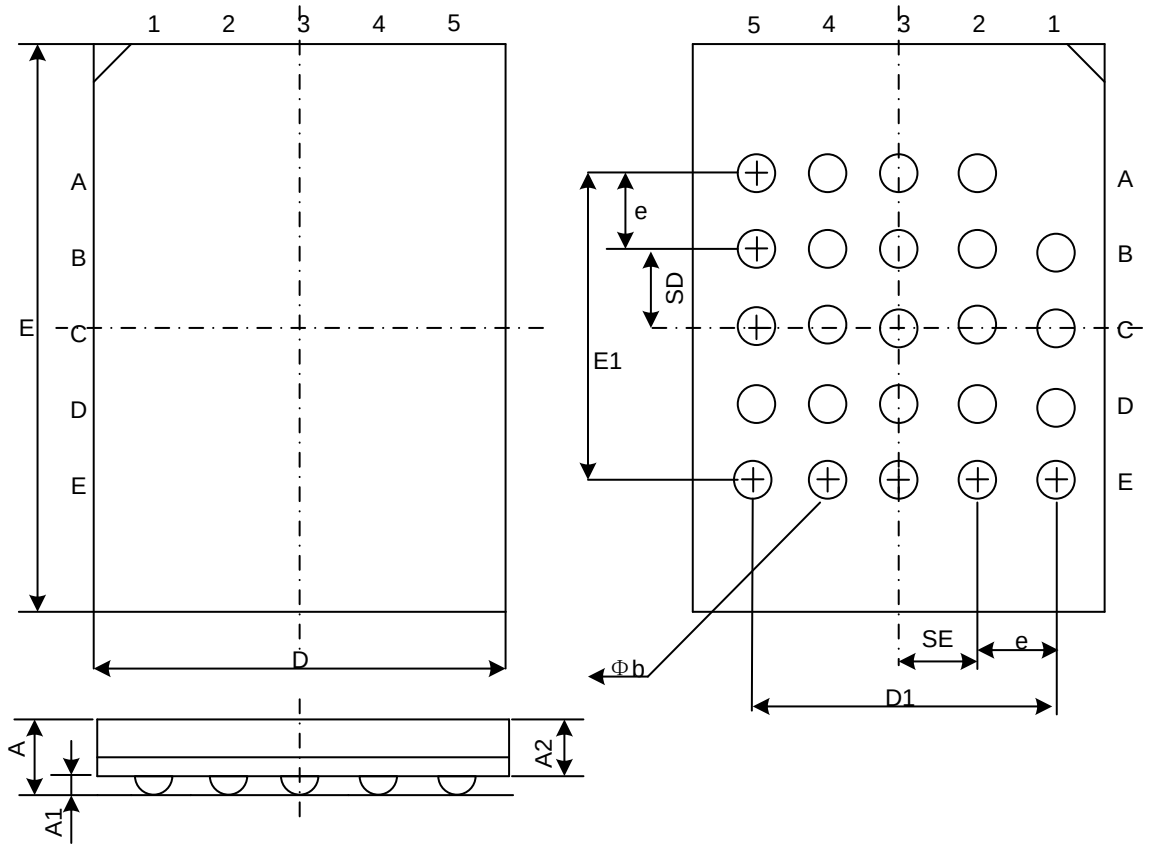
Figure 26-2. WSON8 (6*5mm)



Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	5.90	3.30	4.90	3.90	1.27	0.50
	Nom	0.75	0.02	0.203	0.40	6.00	3.40	5.00	4.00		0.60
	Max	0.80	0.05	0.250	0.50	6.10	3.50	5.10	4.10		0.75
Inch	Min	0.028	0	0.007	0.014	0.232	0.130	0.193	0.154	0.05	0.020
	Nom	0.030	0.001	0.008	0.016	0.236	0.134	0.197	0.157		0.024
	Max	0.032	0.002	0.010	0.020	0.240	0.138	0.201	0.161		0.030

Figure 26-3 TFBGA-24 6x8 BALL (5*5-1 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	SE	SD
mm	Min		0.25	0.75	0.35	5.90	4.00 BSC	7.90	4.00 BSC	1.00 BSC	1.00 TYP	1.00 TYP
	Nom		0.30	0.80	0.40	6.00		8.00				
	Max	1.20	0.35	0.85	0.45	6.10		8.10				
Inch	Min		0.010	0.030	0.014	0.232	0.157 BSC	0.311	0.157 BSC	0.039 BSC	0.039 TYP	0.039 TYP
	Nom		0.012	0.031	0.016	0.236		0.315				
	Max	0.047	0.014	0.033	0.018	0.240		0.319				

27 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial Release		2025-3-28

Important Notice

This document is the property of GigaDevice Semiconductor (Beijing) Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company under the intellectual property laws and treaties of the People’s Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it’s suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it’s suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products. Customers shall discard the device according to the local environmental law.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Products and services described herein at any time, without notice.