GigaDevice Semiconductor Inc.

GD32H7xx Power Bypass Mode User Guide

Application Note
AN225

Revision 1.1

（Feb. 2025）

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1. Introduction

This article is specifically designed for engineering personnel developing the GD32H7xx series, mainly introducing the usage methods, precautions, and peripheral component selection for the GD32H7xx power bypass mode. With the development of semiconductor technology, the integration of internal circuits in chips is getting higher and higher, which brings with it an increase in the heat generation density of the chips. As the junction temperature (TJ) of the chip increases, the lifespan of the device will decrease, and the failure rate will also increase accordingly. The GD32H7xx, as a high-performance product of GD32, requires special attention to the high power consumption and heat generation that come with its use. When designing the chip, this product has reserved a power bypass mode, which allows direct power supply to the internal core domain of the MCU from an external power source, avoiding the heat generation caused by the use of internal LDO in extreme environments, which could lead to thermal runaway of the chip.

This article primarily introduces the usage methods, precautions, and peripheral component selection for the GD32H7xx power bypass mode.

2. Introduction to Power Bypass Mode

In this mode, the internal SMPS and LDO of the chip are turned off, and the external circuit supplies power to the $V_{0.9V}$ domain (core domain) through the VCORE pin. On different packages of the H7 series, the routing of the SMPS pins varies. The BGA176 and LQFP176 packages include the SMPS module, and their SMPS-related pins and VDDLDO pins are both routed out on the package; the LQFP144, LQFP100, and BGA100 packages do not include the SMPS module, and there are no related pins on the package. Therefore, the circuit connection when operating in bypass mode is slightly different, and the specific circuit can refer to ***Figure 2-1. Bypass Mode (with SMPS Module)*** and ***Figure 2-2. Bypass Mode (without SMPS Module)*** design (when the SMPS module is turned off, the VDDSMPS pin must be connected to VDD or VSS).

Figure 2-1. Bypass Mode (with SMPS Module)

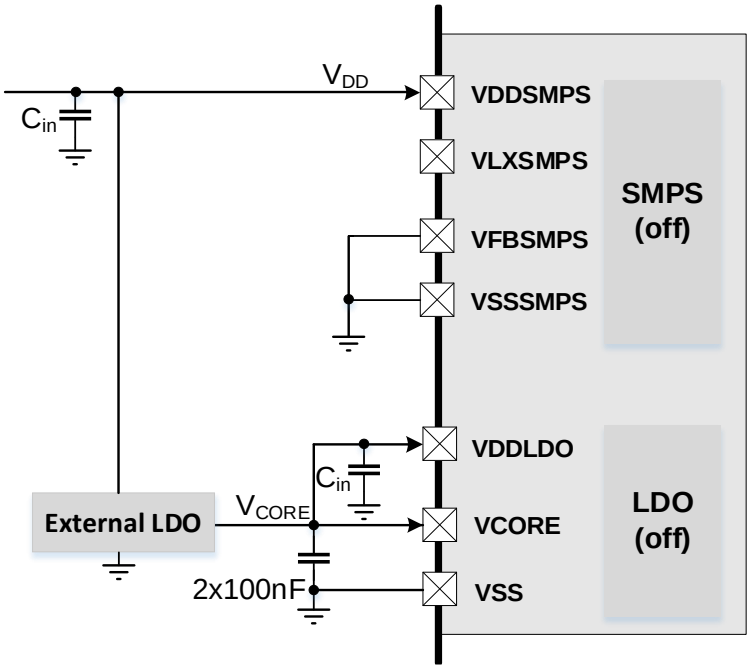
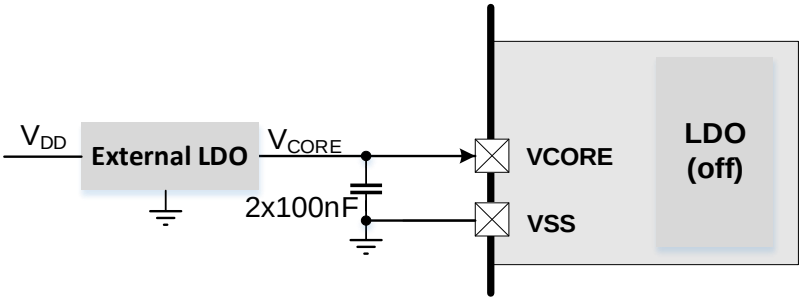


Figure 2-2. Bypass Mode (without SMPS Module)



The configuration method to enter this power supply mode is as follows: the DVSEN bit is set to 0b0, the values of DVSCFG and DVSVC[1:0] have no effect, and the SMPS buck regulator is in the off state; the LDOEN bit is set to 0b0, and the LDO is in the off state; the BYPASS bit is set to 0b1, and the $V_{0.9V}$ domain is powered by the VCORE pin. The register configuration

for the output voltage of the SMPS and LDO is shown in ***Table 2-1. Bypass Mode register configuration table***:

Table 2-1. Bypass Mode register configuration table

Symbol	Description
DVSEN	0：SMPS disable
LDOEN	0：LDO disable
BYPASS	1：BYPASS enable

Note: When using the bypass mode for power supply, make sure to switch the power supply mode to bypass mode in the software immediately after the chip initialization；otherwise, there are unforeseeable risks. When programming with the "GD32H7xx_Firmware_Library", make settings in the "system_gd32h7xx.c" file, as shown in ***Figure 2-3. The software is set to bypass mode***.

Figure 2-3. The software is set to bypass mode

```
#if defined(GD32H7XXI)
//#define SEL_PMU_SMPS_MODE    PMU_DIRECT_SMPS_SUPPLY
//#define SEL_PMU_SMPS_MODE    PMU_LDO_SUPPLY
#define SEL_PMU_SMPS_MODE    PMU_BYPASS
#elif defined(GD32H7XXZ) | defined(GD32H7XXV)
//#define SEL_PMU_SMPS_MODE    PMU_LDO_SUPPLY
#define SEL_PMU_SMPS_MODE    PMU_BYPASS
#endif
```

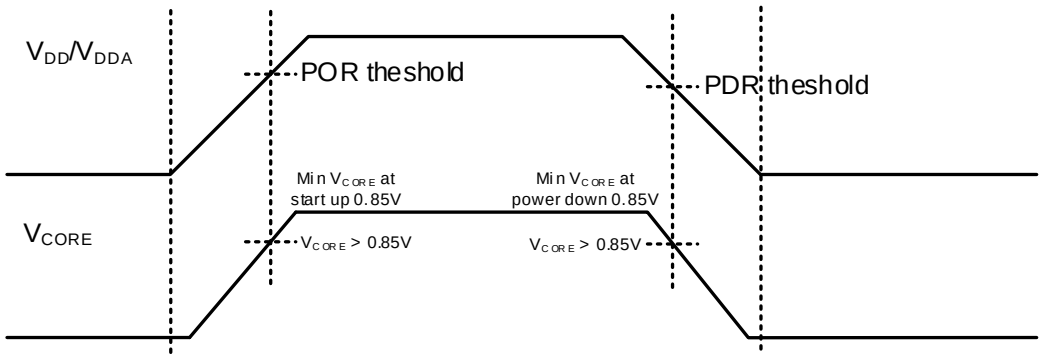
```
#if defined (SEL_PMU_SMPS_MODE)
    /* power supply config */
   pmu_smps_ldo_supply_config(SEL_PMU_SMPS_MODE);
#endif

    /* configure system clock */
    system_clock_config();
```

Note: It is recommended to complete the switching of the power mode before configuring the system clock.

3. Power-up and Power-down Sequence

The power-up and power-down sequence requirements for the power bypass mode are as illustrated in ***Figure 3-1. Bypass Mode power-up and power-down timing diagram***.

Figure 3-1. Bypass Mode power-up and power-down timing diagram

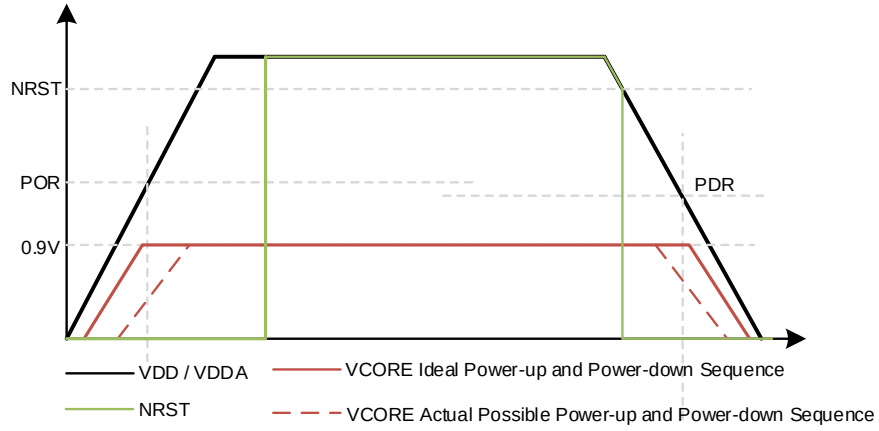


Note：

1. Before the MCU's V_{DD}/V_{DDA} voltage rises to the POR (Power-On Reset) threshold, ensure that the V_{CORE} voltage is greater than 0.85 V.
2. Before the MCU's V_{DD}/V_{DDA} voltage drops to the PDR (Power-Down Reset) threshold, ensure that the V_{CORE} voltage is greater than 0.85 V.
3. Under any operating condition, ensure that the V_{DD}/V_{DDA} voltage is greater than the V_{CORE} voltage.
4. Be sure to pull the PDR_ON pin up to VDD to enable the internal POR / PDR function. For details, please refer to the "AN109 GD32H7xx Series Hardware Development Guide."

If the external power supply design makes it difficult to meet the timing requirements, a reset chip can be added to avoid the power-up and power-down times, as shown in ***Figure 3-2. Using reset chip to avoid inappropriate power-up and power-down timing*** The reset chip needs to ensure that VDD / VDDA and VCORE are stable before pulling up during power-up, and to pull down before VCORE drops during power-down. Additionally, the minimum operating voltage of the reset chip should be lower than the Power-Down Reset (PDR) threshold.

Figure 3-2. Using reset chip to avoid inappropriate power-up and power-down timing



4. Selection of External Power Supply

4.1. Using LDO for Power Supply

Considering power supply stability and ease of controlling the power-up and power-down sequences, it is generally recommended to use an external LDO for power supply in bypass mode. To easily meet the power-up and power-down sequence requirements, the following points are suggested when selecting and using an LDO：

1. The input of the LDO is connected to the V_{DD} terminal.
2. The minimum operating input voltage of the LDO, LDO_VIN_{min}, should be less than the MCU's Power-On Reset (POR) and Power-Down Reset (PDR) voltages. The minimum dropout voltage of the LDO plus 0.85V should be less than the MCU's POR and PDR voltages.
3. The enable control voltage of the LDO, VEN_H_{min}, should be less than the MCU's POR, and VEN_L_{max} should be less than the MCU's PDR.

Note: For the GD32H7xx MCU, POR = 1.53 V, and PDR = 1.48 V. For detailed information, refer to the datasheet.

Using the GD30LD1002x as an external power supply for the VCORE pin of the GD32H7xx, the relevant parameters are as shown in ***Table 4-1. GD30LD1002x Datasheet (Excerpt)***：

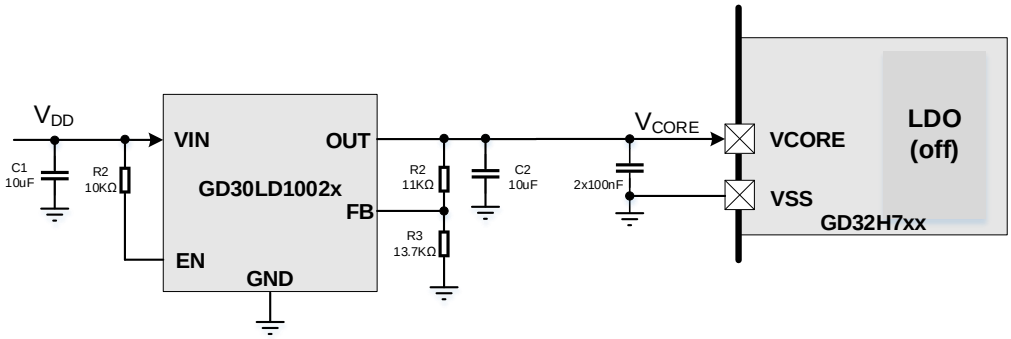
Table 4-1. GD30LD1002x Datasheet (Excerpt)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Range	–	1.4	–	6.5	V
V_{OUT}	Output Voltage Range	–	0.5	–	5.2	V
V_{DROP}	Dropout Voltage	V_{IN} = 1.4 V, I_{OUT} =1.2 A	–	90	150	mV
V_{EN_H}	EN Pin High-Level	–	1.1	–	6.5	V
V_{EN_L}	EN Pin Low-Level	–	0	–	0.5	V

Its minimum input voltage is 1.4 V, VEN_H_{min} = 1.1 V, VEN_L_{max} = 0.5 V, supports 0.9 V output, and the maximum output can reach 1.2 A, which meets the selection requirements. For more details, please refer to **www.gigadevice.com**.

The circuit schematic is as shown in ***Figure 4-1. Using LDO to supply power to VCORE schematic diagram***:

Figure 4-1. Using LDO to supply power to VCORE schematic diagram



Powering VCORE with this chip, the power-up and power-down timing sequences are as shown in ***Figure 4-2. The power-up sequence for supplying power to VCORE using LDO*** , ***Figure 4-3. The power-down sequence for supplying power to VCORE using LDO***, and it can be observed that the power-up and power-down timing sequences can meet the specified requirements.

Figure 4-2. The power-up sequence for supplying power to VCORE using LDO

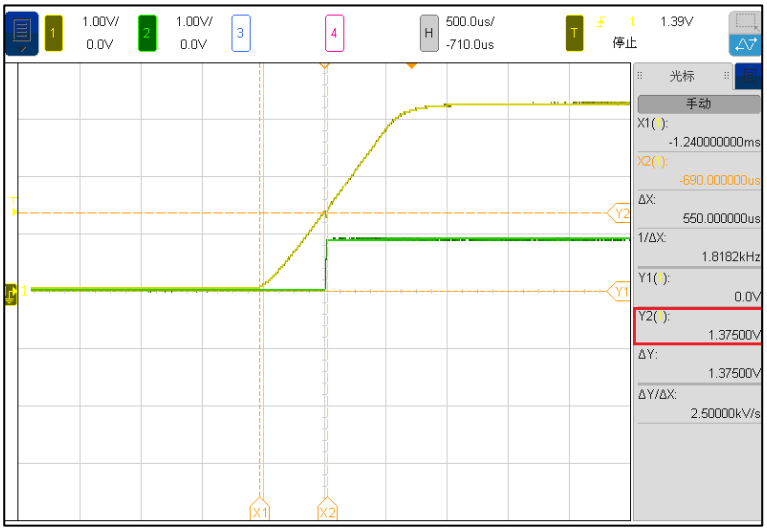
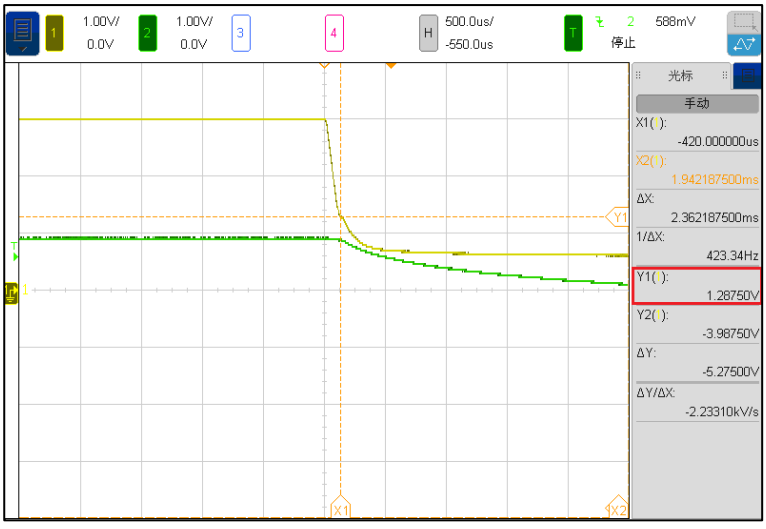


Figure 4-3. The power-down sequence for supplying power to VCORE using LDO



Note: If the VDD power-up speed is too fast, it may also cause the power-up sequence to not meet the requirements.

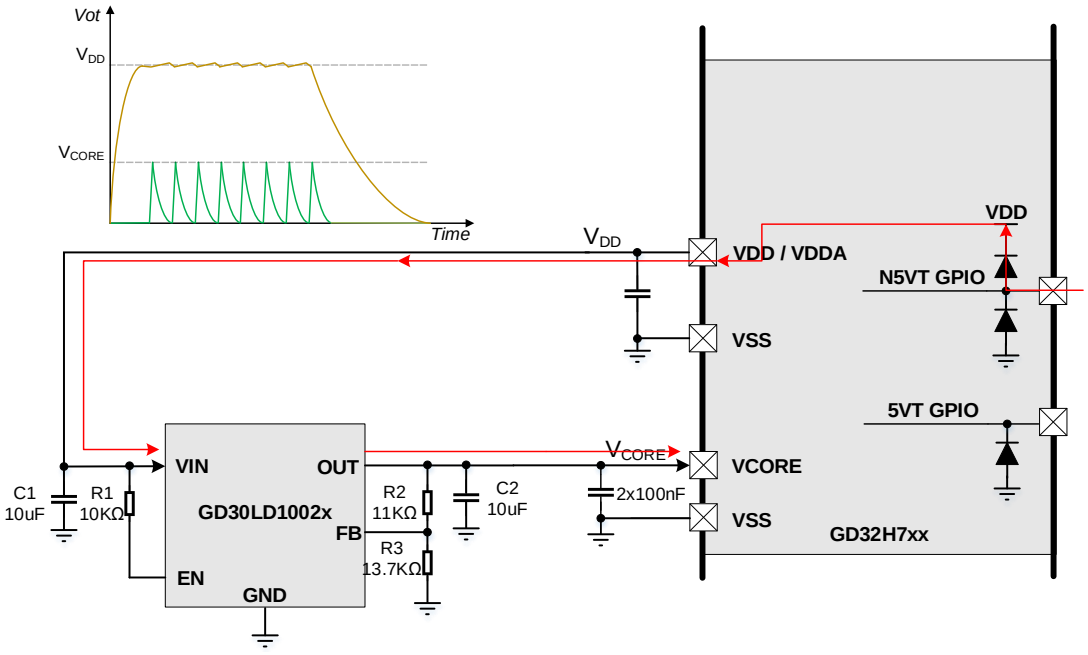
4.2. The Impact of GPIO on Power Bypass Mode

The GPIO of GD32H7xx is divided into 5VT and N5VT, with one difference being that N5VT has pull-up protection diodes to VDD. For more details, you can refer to “AN092 GD32 MCU GPIO structure and precautions”.

When using the power bypass mode, during the power-up and power-down stages of the MCU or during power loss, if the N5VT GPIO still has level driving, current may flow from the outside through the internal pull-up diodes to VDD, and then to the external LDO to generate VCORE voltage. If the driving current is insufficient or the voltage reached by leakage is at the critical value for LDO startup, it may cause the external LDO to not start stably, resulting in oscillation of its output VCORE voltage. As shown in ***Figure 4-4. Leakage current in GPIO causes oscillation in VCORE voltage***

This is an unstable state. If at this time the VDD voltage is greater than the POR threshold, the chip will start up, but if the VCORE core voltage is unstable, it can lead to unpredictable risks. In many usage scenarios, the MCU GPIO periphery will use diode protection circuits, which can also cause such situations to occur.

Figure 4-4. Leakage current in GPIO causes oscillation in VCORE voltage



Considering this, it is important to avoid the situation where GPIO leakage to VDD occurs due to GPIO being driven by a level during the MCU's power-up and power-down stages or during power loss.

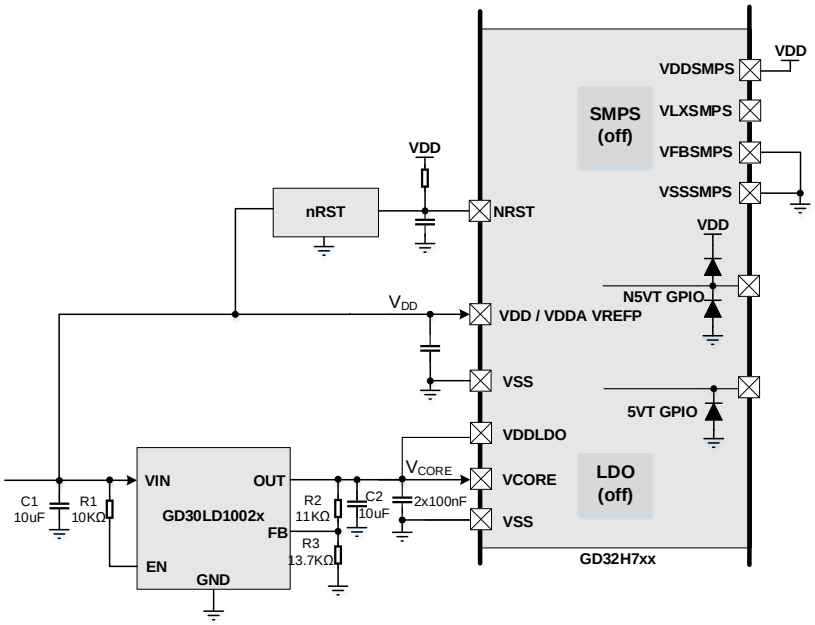
4.3. Optimization Schemes for Power Bypass Mode

For the above-mentioned leakage issue, it is required to always follow the Datasheet's specified maximum GPIO input voltage not exceeding VDD + 0.3 V and an input current of 0. If the related issues cannot be avoided under working conditions, the following solution options can be selected for optimized design.

4.3.1. Use reset chip solution.

A reset chip can be added to the VDD terminal to ensure that when the voltage leaked to VDD is below the reset threshold, NRST can be pulled low directly to avoid malfunction. Additionally, it can also circumvent non-compliant power-up and power-down sequences, as shown in ***Figure 4-5. Use a reset chip to prevent misoperation***. The reset chip should be chosen with an open-drain output to avoid affecting the MCU's own reset actions in other scenarios. The minimum operating voltage of the reset chip should be lower than the PDR, to prevent NRST from being pulled back up after the reset chip powers down during shut-off. The monitoring voltage is generally advisable to be 90% of VDD; for example, if VDD = 3.3 V, a reset chip of 3.08 V or 2.93 V can be selected.

Figure 4-5. Use a reset chip to prevent misoperation



5. Precautions for Using External Power Supplies

1. The input voltage range for V_{CORE} is 0.873 V to 0.955 V, so it should be ensured that the typical value is 0.9 V, and the power supply ripple should be below 50 mV. Even in harsher application scenarios, the power supply fluctuation range should also be ensured to be within 50 mV.
2. It is recommended that the load capacity of external components should be greater than 600 mA, and in extreme environments, it should be considered to use no less than 800 mA. Moreover, the output voltage fluctuation range under different loads should also meet the aforementioned requirement of 50 mV.
3. The ESR effect of PCB traces and the IR drop with high current, when routing PCB traces, it is necessary to consider widening the trace width from the external power supply to the VCORE pin to reduce ESR, ensuring that the voltage at the chip's VCORE pin meets the amplitude and fluctuation requirements.

6. Revision history

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Dec.18, 2024
1.1	1、Add instructions for software switching in Chapter 2. 2、Add an explanation in Chapter 3 about pulling PDR_ON up to VDD. 3、Add a description of power-up speed in Section 4.1 summary.	Feb.27.2025

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