Zero-Drift, Micro-Power 1.5MHz, RRIO Operational Amplifiers

1 Features

- High DC Precision:
  – 8μV (maximum) VOS with a Drift of ±40 nV/°C(maximum)
  – A_{VOL}: 112dB (minimum, V_{DD} = 5.5V)
  – PSRR: 112dB (minimum, V_{DD} = 5.5V)
  – CMRR: 112dB (minimum, V_{DD} = 5.5V)
  – V_n: 0.45μV_{PP} (typical, f = 0.1 to 10Hz)
- 1.5MHz Bandwidth and 1.2V/μs Slew Rate
- Settling Time to 0.1% with 1V Step: 1.2μs
- Overload Recovery Time to 0.1%: 35μs
- Micro-Power 125μA per Amplifier and 1.8V to 5.5V Wide Supply Voltage Range
- Operating Temperature Range: −40°C to +125°C

2 Applications

- Precision Current Sensing
- Resistor Thermal Detectors
- Temperature, Position and Pressure Sensors
- Medical Equipment
- Electronic Scales
- Strain Gage Amplifiers
- Thermocouple Amplifiers
- Driving A/D Converters

3 Description

The GD30AP855x family of amplifiers provides input offset voltage correction for very low offset and drift through the use of patented fast step response chopper stabilized techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of 1/f noise. This design breakthrough allows the combination of a gain bandwidth product of 1.5MHz and a high slew rate of 1.2V/μs, while only drawing 125μA supply current. These devices are unity gain stable and have good Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR).

The GD30AP855x series are perfectly suited for applications that require precision amplification of low level signals, in which error sources cannot be tolerated, even in which high bandwidth and fast transition are needed. The rail-to-rail input and output swings make both high-side and low-side sensing easy. The GD30AP855x series can operate with a single supply voltage as low as 1.8V for 2-cell battery applications.

The GD30AP855x op-amps have enhanced EMI protection to minimize any electromagnetic interference from external sources, and have high electro-static discharge (ESD) protection (5-kV HBM). All models are specified over the extended industrial temperature range of −40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AP8551	SOT23-5L	2.92mm x 1.63mm
	SOIC-8L	4.90mm x 3.92mm
GD30AP8552	DFN2x2-8L	2.00mm x 2.00mm
	SOIC-8L	4.90mm x 3.92mm
	MSOP-8L	3.00mm x 3.00mm
GD30AP8553	SOT23-5L	2.92mm x 1.63mm
	SC70-5L	2.10mm x 1.25mm

1. For all available packages, see the *Package Information* and *Ordering Information* at the end of datasheet.

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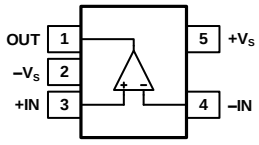
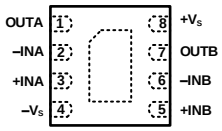
4 Device Overview

4.1 Pinout and Pin Assignment

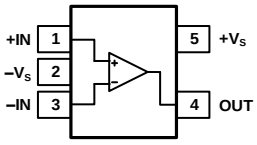
GD30AP8551
SOT23-5L
Top View



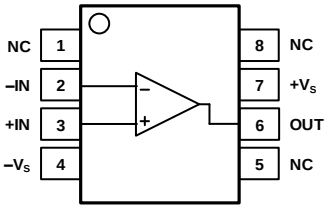
GD30AP8552
DFN2x2-8L
Top View



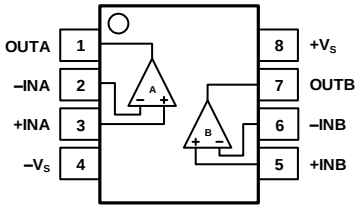
GD30AP8553
SOT23-5L / SC70-5L
Top View



GD30AP8551
SOIC-8 / MSOP-8
Top View



GD30AP8552
SOIC-8 / MSOP-8
Top View



4.2 Pin Description

PIN NUMBER / NAME	PIN TYPE[1]	FUNCTION
-IN	I	Inverting input of the amplifier. The voltage range is from (V_{S-} – 0.1V) to (V_{S+} + 0.1V).
+IN	I	Non-inverting input of the amplifier. This pin has the same voltage range as –IN.
$+V_S$	P	Positive power supply. The voltage is from 2.0 V to 5.5 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 2.0 V to 5.5 V.
$-V_S$	P	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 2.0 V to 5.5 V.
OUT	O	Amplifier output.

1. I = Input, O = Output, P = Power.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{S+} to V_{S-}	Supply Voltage, V_{S+} to V_{S-}		10.0	V
V_I	Signal Input Voltage	V_{S-} − 0.5	V_{S+} + 0.5	V
I_I	Signal Input Current	−10	10	mA
	Output Short-Circuit		Continuous	s
T_J	Junction Temperature, T_J		150	°C
T_{stg}	Storage Temperature Range, T_{stg}	−65	+150	°C
	Lead Temperature Range (Soldering 10 sec)		260	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_S	Input supply voltage range(T_A= 0°C to +70 °C)	1.8		5.5	V
	Input supply voltage range(T_A= –40°C to +70 °C)	2.0		5.5	V
V_{CM}	Common-mode voltage range	V_{S-} − 0.1		V_{S+} + 0.1	V
T_A	Operating temperature range	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±5000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±2000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Characteristics

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Package Thermal Resistance	SC70-5L	333	°C/W
		SOT23-5L	190	
		DFN2x2-8L	94	
		MSOP-8L	201	
		TSSOP-8L	160	
		SOIC-8L	125	

Thermal Characteristics(continued)

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Package Thermal Resistance	TSSOP-14L	112	°C/W
		SOIC-14L	115	

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_S = 5.0V, V_{CM} = V_S/2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, T_A = +25°C, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±2	±8	μV
dV_{OS}/d_T	Offset voltage drift[1]	T_A = −40 to +125°C		±5	±40	nV/°C
PSRR	Power supply rejection ratio	V_S = 2.0 to 5.5 V, V_{CM} < V_{S+} − 2V	112	126		dB
		T_A = −40 to +125°C	106			
INPUT BIAS CURRENT						
I_B	Input bias current[1]			±70		pA
		T_A = +85°C		±150		
		T_A = +125°C		±700		
I_{OS}	Input offset current[1]			±100		pA
NOISE						
V_n	Input voltage noise	f = 0.01 to 1 Hz		0.1		uV_{P-P}
		f = 0.1 to 10 Hz		0.45		
e_n	Input voltage noise density	f = 1 KHz		15		nV/√Hz
		f = 10 KHz		19		
I_n	Input current noise density	f = 1 KHz		10		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		V_{S-} – 0.1		V_{S-} + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, V_{CM}= −0.1 to 5.5 V	112	130		dB
		V_{CM} = 0 to 5.3 V, T_A= −40 to +125°C	106			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.0 V	102	122		
		V_{CM} = 0 to 1.8 V, T_A= −40 to +125°C	96			
INPUT IMPEDANCE						
R_{IN}	Input resistance		100			GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		

Electrical Characteristics

V_S = 5.0V, V_{CM} = V_S/2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, T_A = +25°C, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{VOL}	Open-loop voltage gain	R_L = 20 kΩ, V_O = 0.05 to 3.5 V	112	132		dB
		T_A = −40 to +125°C	106			
		R_L = 2KΩ, V_O = 0.15 to 3.5 V	101	120		
		T_A = −40 to +125°C	95			
FREQUENCY RESPONSE						
GBW	Gain band width product			1.5		MHz
SR	Slew rate	G = +1,CL= 100pF, V_O = 1.5 to 3.5 V		1.2		V/μs
t_S	Settling time	To 0.1%, G = +1, 1V step		1.2		μs
		To 0.01%, G = +1, 1V step		1.5		
t_{OR}	Overload recovery time	VIN* Gain > V_S		35		μs
OUTPUT						
V_{OH}	High output voltage swing	R_L= 20KΩ		V_{S+} − 6		mV
		R_L= 2KΩ	V_{S+} − 100	V_{S+} − 60		
V_{OL}	Low output voltage swing	R_L= 20kΩ		V_{S-} + 4		mV
		R_L= 2KΩ		V_{S-} + 40	V_{S-} + 66	
Z_{OUT}	Open-loop output impedance	f = 350 kHz, I_O = 0		2		kΩ
I_{SC}	Short-circuit current	Source current through 10Ω		40		mA
		Sink current through 10Ω		50		
POWER SUPPLY						
V_S	Operating supply voltage	T_A = 0°C to +70°C	1.8		5.5	V
		T_A = −40°C to +125°C	2.0		5.5	
I_Q	Quiescent current (per amplifier)		80	125	190	μA

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

V_S = ±2.5V, V_{CM} = V_S /2, R_L = 10kΩ connected to V_S /2, and C_L = 100pF, at T_A = +25°C, unless otherwise noted.

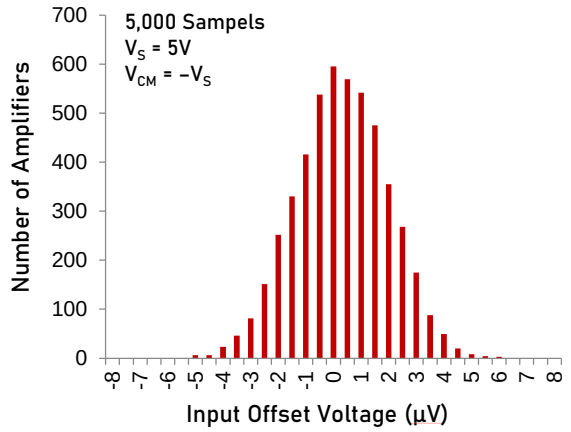


Figure 1. Offset Voltage Production Distribution

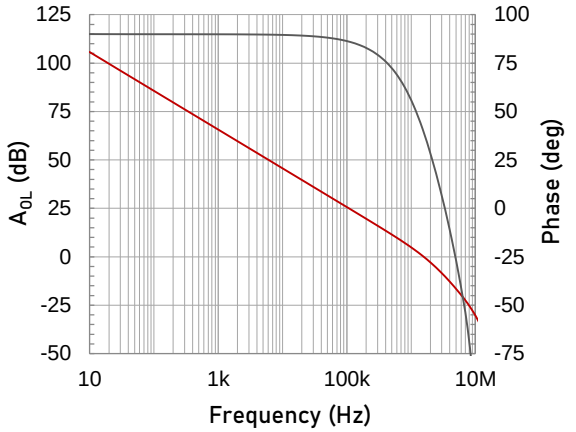


Figure 2. Open Loop Gain and Phase vs. Frequency

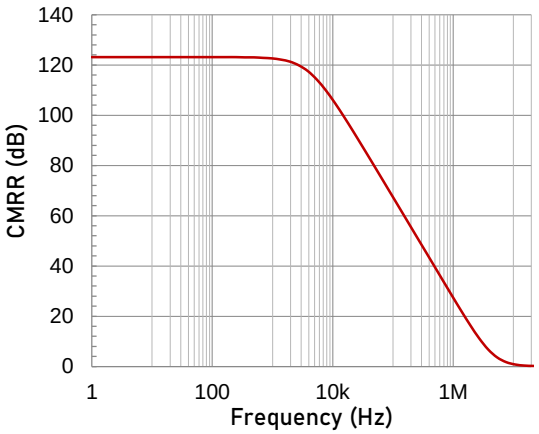


Figure 3. Common Mode Rejection Ratio vs. Frequency

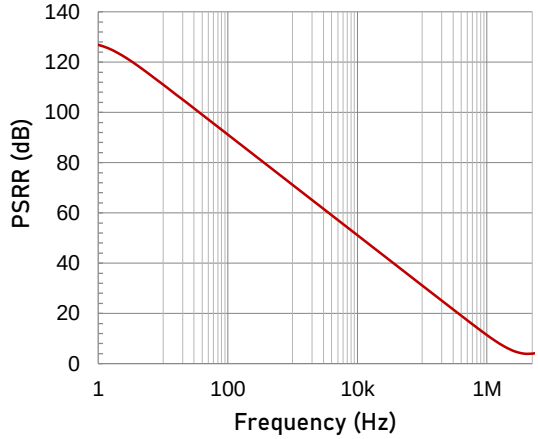


Figure 4. Power Supply Rejection Ratio vs. Frequency

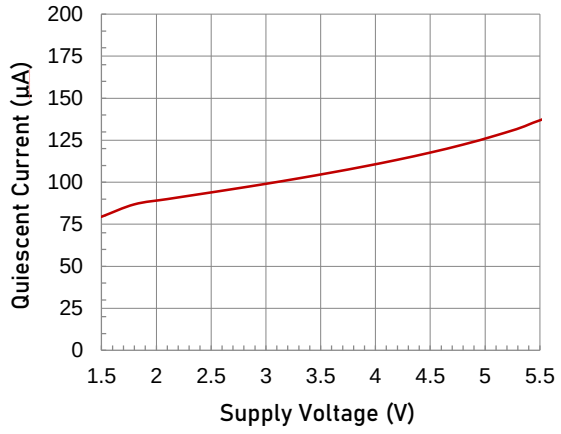


Figure 5. Quiescent Current vs. Supply Voltage

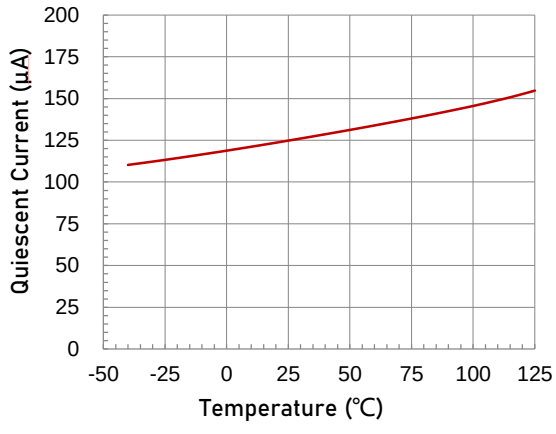


Figure 6. Quiescent Current vs. Temperature

Typical Characteristics (continued)

V_S = ±2.5V, V_{CM} = V_S /2, R_L = 10kΩ connected to V_S /2, and C_L = 100pF, at T_A = +25°C, unless otherwise noted.

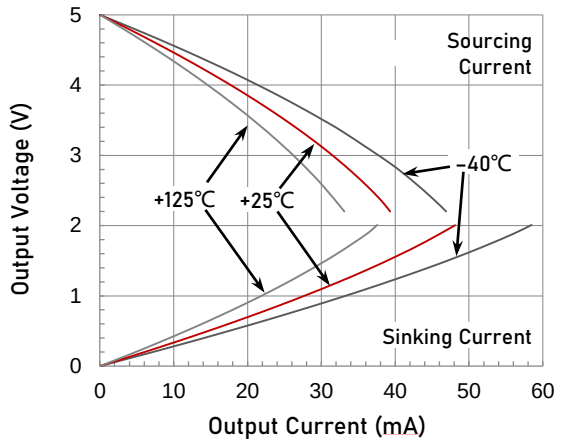


Figure 7. Output Voltage Swing vs. Output Current

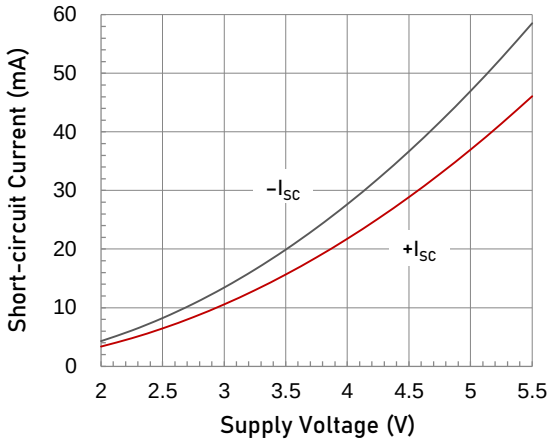


Figure 8. Short-circuit Current vs. Supply Voltage

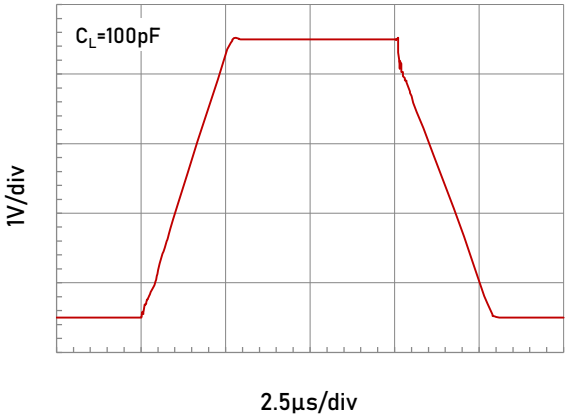


Figure 9. Large Signal Step Response(4V step)

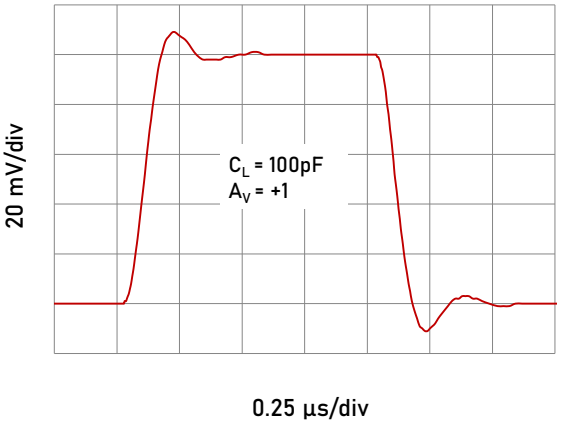


Figure 10. Small Signal Step Response(0.1 step)

6 Functional Description

The GD30AP855x operational amplifiers are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto- calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally- generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on materials used.

6.1 Operating Voltage

The GD30AP855x family is fully specified and ensured for operation from 2.0V to 5.5V (±1.0V to ±2.75V). In addition, many specifications apply from −40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages (V_{S+} to V_{S-}) higher than +10V can permanently damage the device.

6.2 Rail-to-Rail Input

The input common-mode voltage range of the GD30AP855x series extends 100mV beyond the negative supply rail and reaches the positive supply rail. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}−1.4V to the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately V_{S+}−1.4V. There is a small transition region, typically V_{S+}−1.2V to V_{S+}−1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}−1.4V to V_{S+}−1.2V on the low end, up to V_{S+}−1V to V_{S+}−0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the GD30AP855x during normal operation is approximately 70pA. In over- driven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

6.3 Input EMI Filter and Clamp Circuit

Figure 11 shows the input EMI filter and clamp circuit. The GD30AP855x op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect

the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of *Absolute Maximum Ratings* for more information.

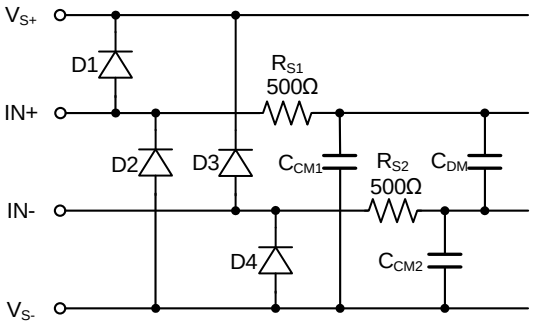


Figure 11. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the GD30AP855x family is composed of two 5kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the −3dB low-pass cutoff frequencies at 35-MHz for common-mode signals, and at 22-MHz for differential signals.

6.4 Rail-to-Rail Output

The GD30AP855x operational amplifiers use an auto-calibration technique with a time-continuous 500kHz operational amplifier in the signal path. This amplifier is zero-corrected every 2μs using a proprietary technique. Upon power up, the amplifier requires approximately 100μs to achieve specified VOS accuracy. This design has no aliasing or flicker noise.

6.5 Capacitive Load and Stability

The GD30AP855x family can safely drive capacitive loads of up to 500pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over- shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the GD30AP855x op-amps must drive a load exceeding 500pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 12. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

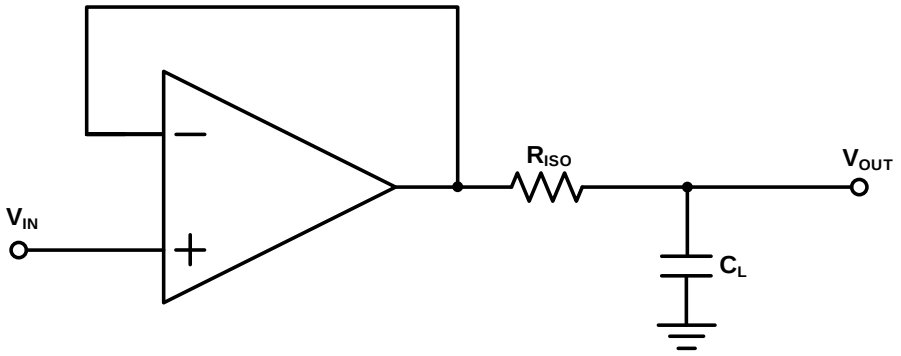


Figure 12. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 13. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

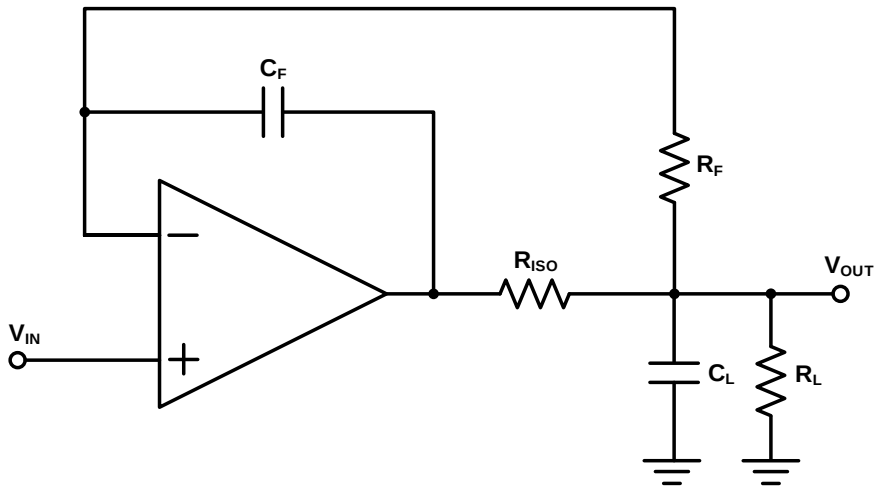


Figure 13. Indirectly Driving Heavy Capacitive Load with DC Accuracy

6.6 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the GD30AP855x family is approximately 35μs.

6.7 EMI Rejection Ratio

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op- amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The GD30AP855x op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \times \log\left(\frac{V_{IN\_PEAK}}{\Delta V_{OS}}\right) \quad (1)$$

6.8 Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

6.9 Maximizing Performance Through Proper Layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the GD30AP855x op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 14 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

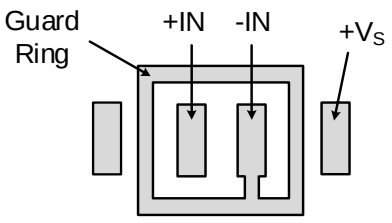


Figure 14. Use a Guard Ring around Sensitive Pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-

component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

7 Application Information

7.1 Precision Low-Side Current Shunt Sensing

Many applications require the sensing of signals near the positive or negative rails. Current shunt sensing is one such application and is mostly used for feedback control systems. It is also used in a variety of other applications, including power metering, battery fuel gauging, and feedback controls in industrial applications. In such applications, it is desirable to use a shunt with very low resistance to minimize series voltage drop. This configuration not only minimizes wasted power, but also allows the measurement of high currents while saving power.

A typical shunt may be 100mΩ. At a measured current of 1A, the voltage produced from the shunt is 100mV, and the amplifier error sources are not critical. However, at low measured current in the 1mA range, the 100μV generated across the shunt demands a very low offset voltage and drift amplifier to maintain absolute accuracy.

The unique attributes of a zero drift amplifier provide a solution. Figure 15 shows a low-side current sensing circuit using the GD30AP855x. The GD30AP855x are configured as difference amplifiers with a gain of 10. Although the GD30AP855x have high CMRR, the CMRR of the system is limited by the external resistors. Therefore, the key to high CMRR for the system is resistors that are well matched from both the resistive ratio and relative drift, where $R_1/R_2 = R_3/R_4$. The transfer function is given by:

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_AMP} = \left(V_{SHUNT} \times I_{LOAD}\right) \times \frac{R_2}{R_1} = 10 \times I_{LOAD} \quad (2)$$

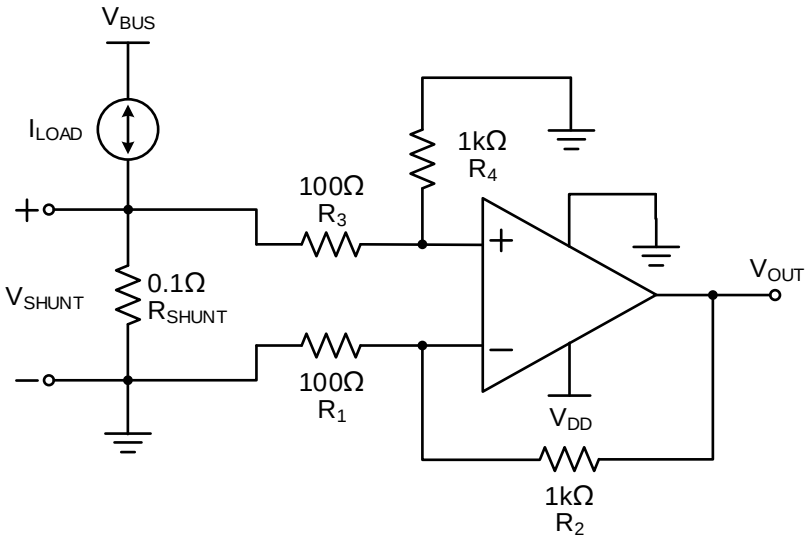


Figure 15. Low Side Current Sensing Circuit

Any unused channel of the GD30AP855x must be configured in unity gain with the input common-mode voltage

tied to the midpoint of the power supplies.

7.2 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1A to +1A. The single-ended output spans from 110mV to 3.19V. This design uses the GD30AP855x because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 16 shows the solution. This solution has the following requirements:

- Supply voltage: 3.3V
- Input: –1A to +1A
- Output: 1.65V±1.54V (110mV to 3.19V)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

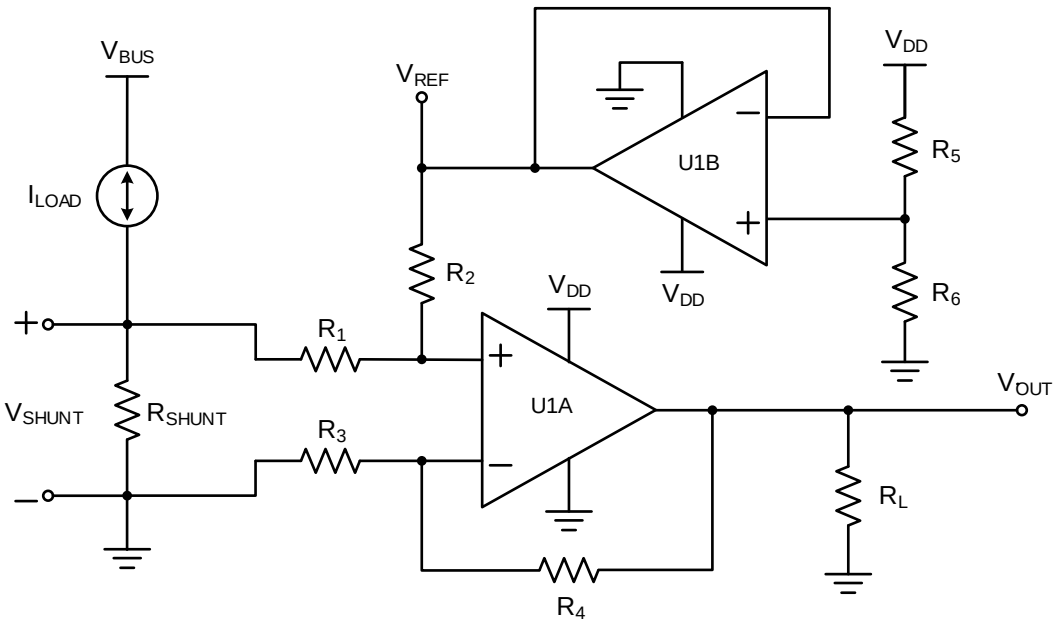


Figure 16. Bidirectional Current-Sensing Schematic

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 3.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_AMP} + V_{REF} \quad (3)$$

Where

$$V_{SHUNT} = I_{LOAD} \times R_{SHUNT} \quad (4)$$

$$Gain_{Diff\_AMP} = \frac{R_4}{R_3} \quad (5)$$

$$V_{REF} = V_{DD} \times \left[R_6 \left(R_5 + R_6 \right) \right] \quad (6)$$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100mV. Equation(7) calculates the maximum value of the shunt resistor given a maximum shunt voltage of 10mV and maximum load current of 1A.

$$R_{SHUNT} = \frac{R_{SHUNT}}{I_{LOAD}} = \frac{100mV}{1A} = 100m\Omega \quad (7)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100mV to +100mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the non-inverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the GD30AP855x, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the GD30AP855x has a typical offset voltage of merely

±2μV (±8μV maximum).

Given a symmetric load current of –1A to +1A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the GD30AP855x must be considered. Equation(8) and Equation(9) depict the typical common-mode range and maximum output swing, respectively, of the GD30AP855x given a 3.3V supply.

$$-100mV < V_{CM} < 3.4V \quad (8)$$

$$-100mV < V_{OUT} < 3.2V \quad (9)$$

The gain of the difference amplifier can now be calculated as shown in Equation(10).

$$Gain_{Diff\_AMP} = \left(V_{OUT\_MAX} - \frac{V_{OUT\_MAX}}{\left[R_{SHUNT} \times (I_{MAX} - I_{MIN}) \right]} \right) = \left(\frac{3.2V - 100mV}{100m\Omega} \right) \times \left[1A - (-1A) \right] = 15.5V / V \quad (10)$$

The resistor value selected for R_1 and R_3 was 1kΩ. 15.4kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors

were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

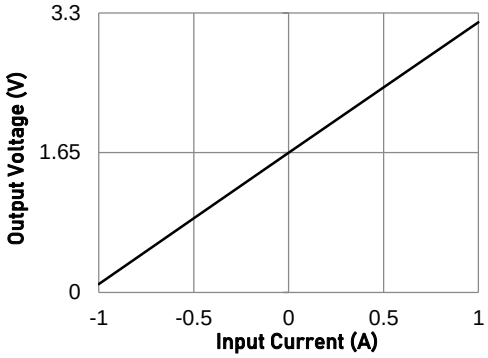


Figure 17. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs. Input Current

7.3 High-Side Voltage-To-Current (V-I) Converter

The circuit shown in Figure 18 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0V to 2V to and output current of 0mA to 100mA.

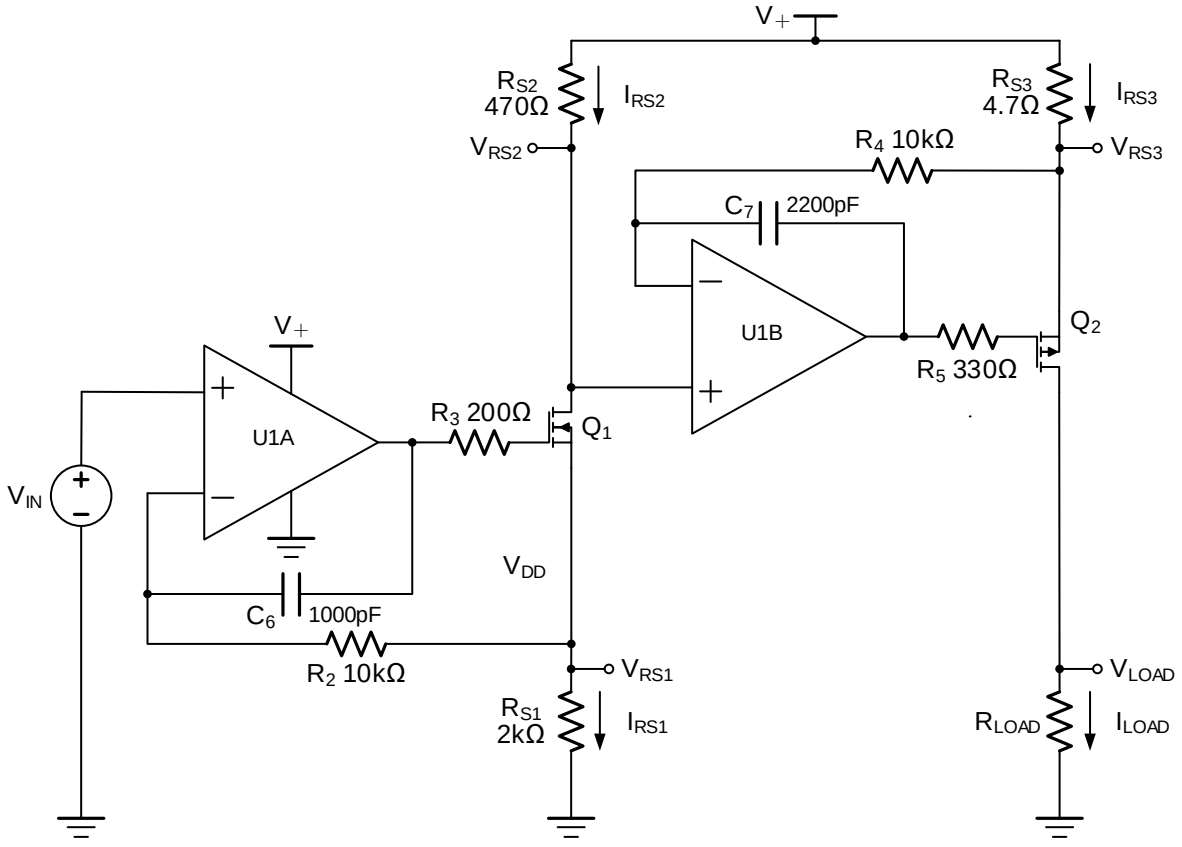


Figure 18. Bidirectional Current-Sensing Schematic

The design requirements are as follows:

- Supply Voltage: 5V DC
- Input: 0V to 2V DC
- Output: 0mA to 100mA DC

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The GD30AP855x CMOS operational amplifier is a high-precision, typically 2μV offset, 5nV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 15mV (at R_L = 10kΩ) of the positive rail. TheGD30AP855x family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of theGD30AP855x ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

Figure 19 shows the measured transfer function for this circuit. The low offset voltage and offset drift of theGD30AP855x facilitate excellent dc accuracy for the circuit.

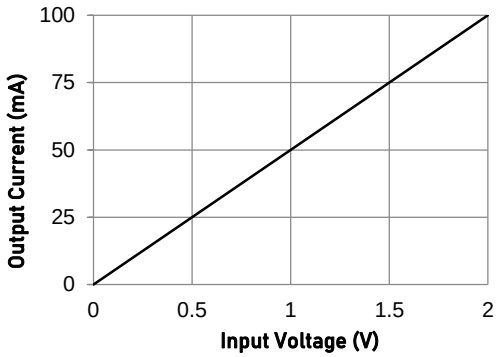


Figure 19. Measured Transfer Function for High-Side V-I Converter

7.4 Single-Supply Instrumentation Amplifier

The extremely low offset voltage and drift, high open-loop gain, high common-mode rejection, and high power supply rejection of the GD30AP855x make them excellent op-amp choices as discrete, single-supply instrumentation amplifiers.

Figure 20 shows the classic 3-op-amp instrumentation amplifier using the GD30AP855x. The key to high CMRR for the instrumentation amplifier are resistors that are well matched for both the resistive ratio and relative drift. For true difference amplification, matching of the resistor ratio is very important, where:

$$\frac{R_5}{R_2} = \frac{R_6}{R_4} \tag{11}$$

$$R_{G1} = R_{G2}, R_1 = R_3, R_2 = R_4, R_5 = R_6 \tag{12}$$

$$V_{OUT} = (V_{IN2} - V_{IN1}) \times \left[1 + \left(\frac{R_1}{R_{G1}}\right)\right] \times \left(\frac{R_5}{R_2}\right) \tag{13}$$

The resistors are important in determining the performance over manufacturing tolerances, time, and temperature. Assuming a perfect unity-gain difference amplifier with infinite common-mode rejection, a 1% tolerance resistor

matching results in only 34dB of common-mode rejection. Therefore, at least 0.01% or better resistors are recommended.

To build a discrete instrumentation amplifier with external resistors without compromising on noise, pay close attention to the resistor values chosen. R_{G1} and R_{G2} each have thermal noise that is amplified by the total noise gain of the instrumentation amplifier and, therefore, a sufficiently low value must be chosen to reduce thermal noise contribution at the output while still providing an accurate measurement.

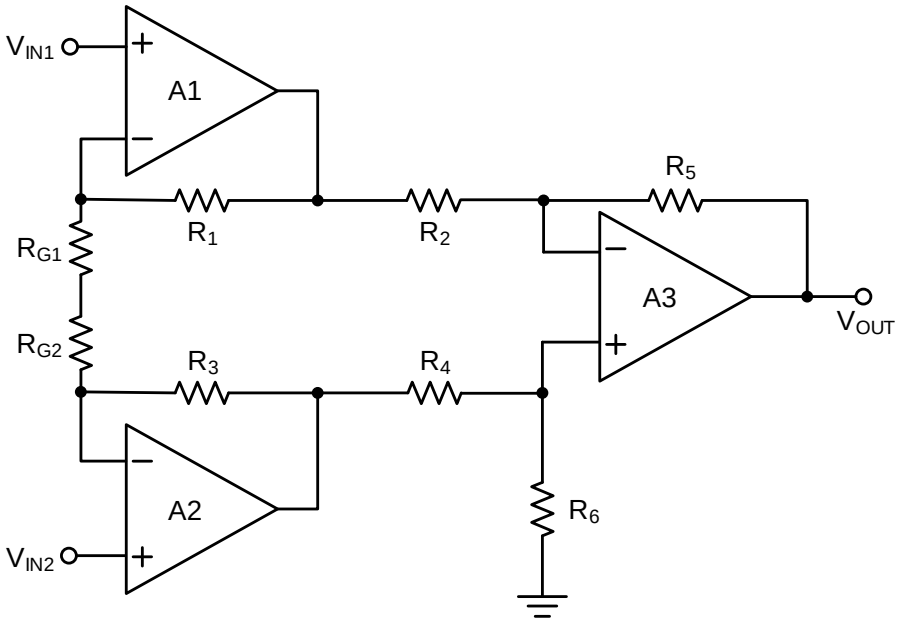


Figure 20. Discrete 3-Op-amp Instrumentation Amplifier

Table 1 shows the external resistors noise contribution referred to the output .

Table 1. Thermal Noise Contribution Example

Resistor	Value(KΩ)	Resistor Thermal Noise (nV/√Hz)	Thermal Noise Referred to Output
R_{G1}	0.4	2.57	128.30
R_{G2}	0.4	2.57	128.30
R_1	10	12.83	25.66
R_2	10	12.83	25.66
R_3	10	12.8	25.66
R_4	10	12.83	25.66
R_5	20	18.14	18.14
R_6	20	18.14	18.14V

Note that A1 and A2 have a high gain of 1 + R1/RG1. Therefore, use a high precision, low offset voltage and low noise amplifier for A1 and A2, such as the GD30AP855x. Conversely, A3 operates at a much lower gain and has a different set of op-amp requirements. Its input noise, referred to the overall instrumentation amplifier input, is divided by the first stage gain and is not as important. Note that the input offset voltage and the input voltage noise of the amplifiers are also amplified by the overall noise gain.

Any unused channel of the GD30AP855x must be configured in unity gain with the input common-mode voltage tied to the midpoint of the power supplies.

Understanding how noise impacts a discrete instrumentation amplifier or a difference amplifier (the second stage

of a 3-op-amp instrumentation amplifier) is important, because they are commonly used in many different applications.

7.5 Load Cell (Strain Gage) Sensor Signal Conditioning

TheGD30AP855x, with its ultralow offset, drift, and noise, is well suited to signal condition a low level sensor output with high gain and accuracy. A weigh scale (load cell) is an example of an application with such requirements. Figure 21 shows a configuration for a single-supply, precision, weigh scale measurement system. TheGD30AP855x is used at the front end for amplification of the low level signal from the load cell.

Current flowing through a PCB trace produces an IR voltage drop; with longer traces, this voltage drop can be several millivolts or more, introducing a considerable error. A1 inch long, 0.005 inch wide trace of 1 oz copper has a resistance of approximately 100mΩ at room temperature. With a load current of 10mA, the resistance can introduce a 1mV error.

Therefore, a 6-wire load cell is used in the circuit. The load cell has two sense pins, in addition to excitation, ground, and two output connections. The sense pins are connected to the high side (excitation pin) and low side (ground pin) of the Wheatstone bridge. The voltage across the bridge can then be accurately measured regardless of voltage drop due to wire resistance. The two sense pins are also connected to the analog-to- digital converter (ADC) reference inputs for a ratio-metric configuration that is immune to low frequency changes in the power supply excitation voltage.

TheGD30AP855x is configured as the first stage of a 3-op-amp instrumentation amplifier to amplify the low level amplitude signal from the load cell by a factor of $1 + 2R_1 / R_G$. Capacitors C_1 and C_2 are placed in the feedback loops of the amplifiers and interact with R_1 and R_2 to perform low-pass filtering. This filtering limits the amount of noise entering the Σ-Δ ADC. In addition, C_3, C_4, C_5, R_3 and R_4 provide further common-mode and differential mode filtering to reduce noise and unwanted signals.

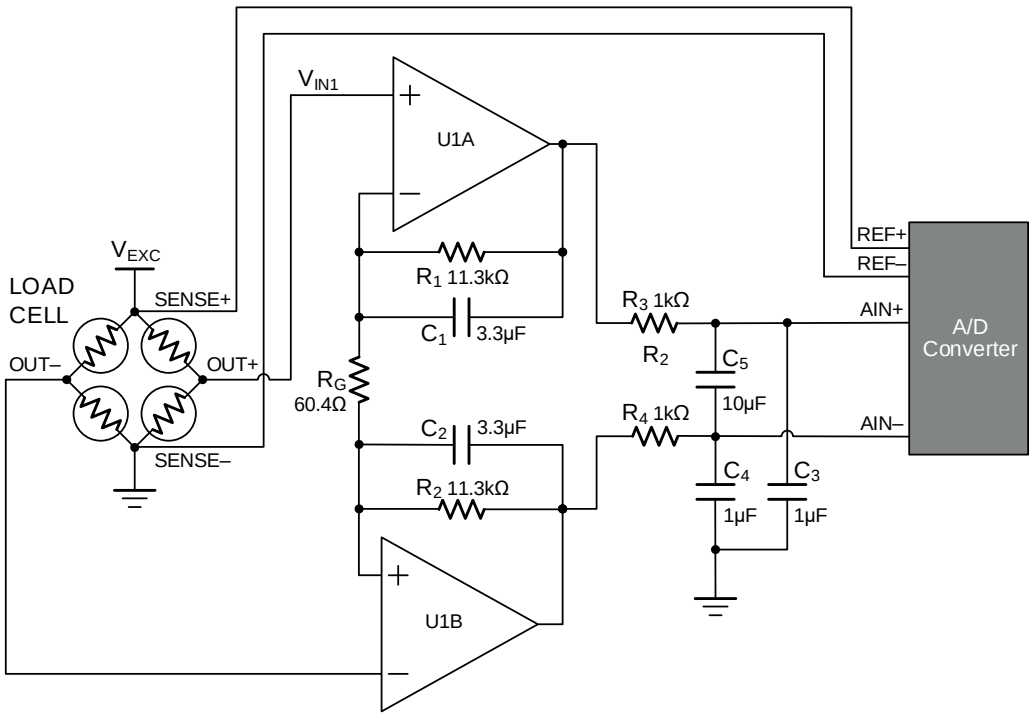
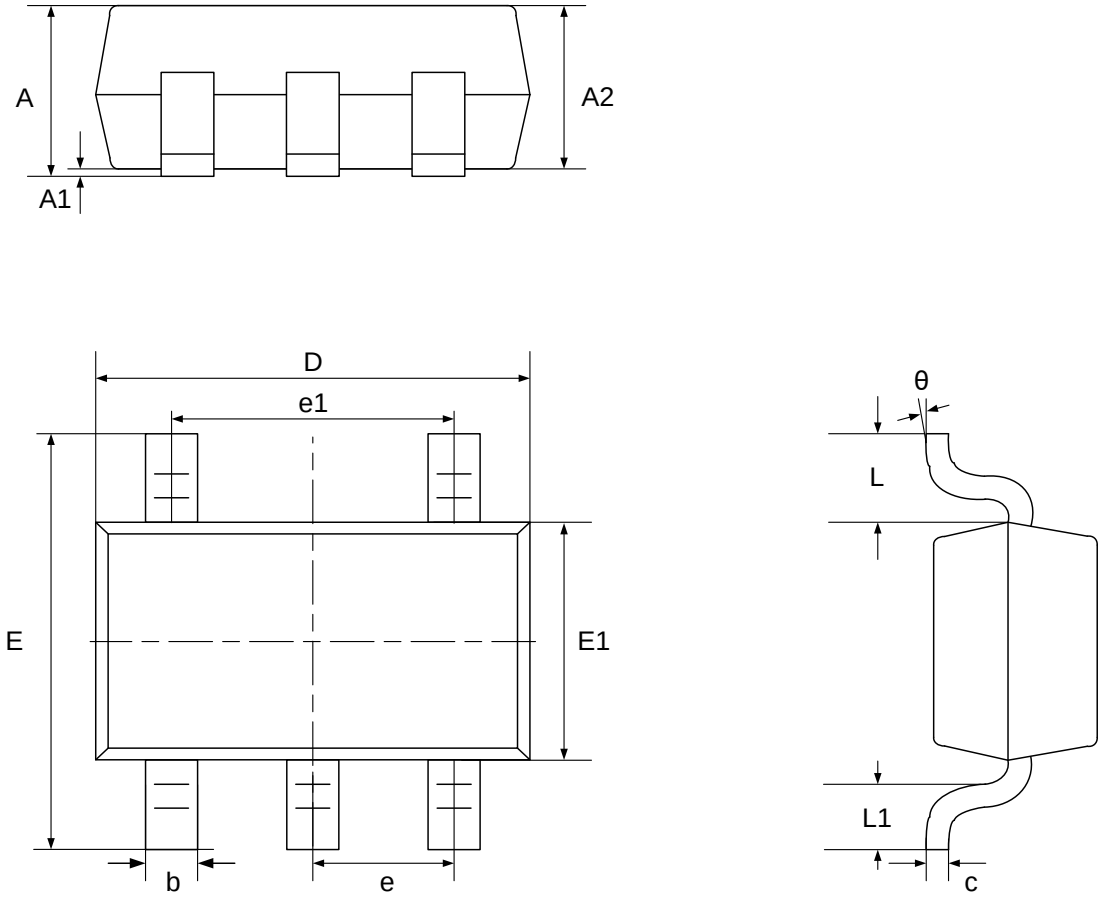


Figure 21. Precision Weigh Scale Measurement System

8 Package Information

8.1 Outline Dimensions

SOT23-5L Package Outline



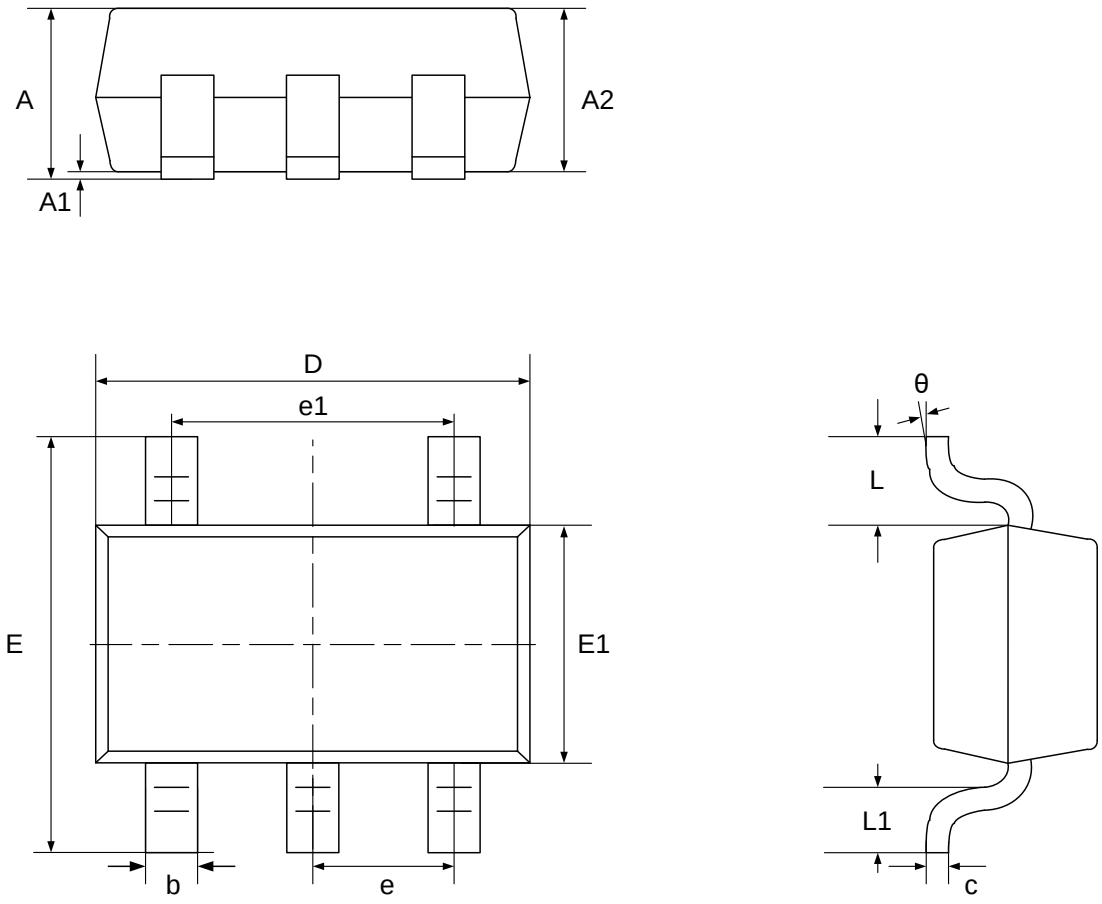
NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 2 *SOT23-5L dimensions(mm)*.

Table 2. SOT23-5L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A			1.35
A1	0.00		0.15
A2	1.00		1.20
b	0.35		0.45
c	0.14		0.20
D	2.82		3.02
E	2.60		3.00
E1	1.526		1.726
e	0.95 BSC		
e1	1.90 BSC		
L	0.60 REF		
L1	0.30		0.60
θ	0°		8°

SC70-5L Package Outline



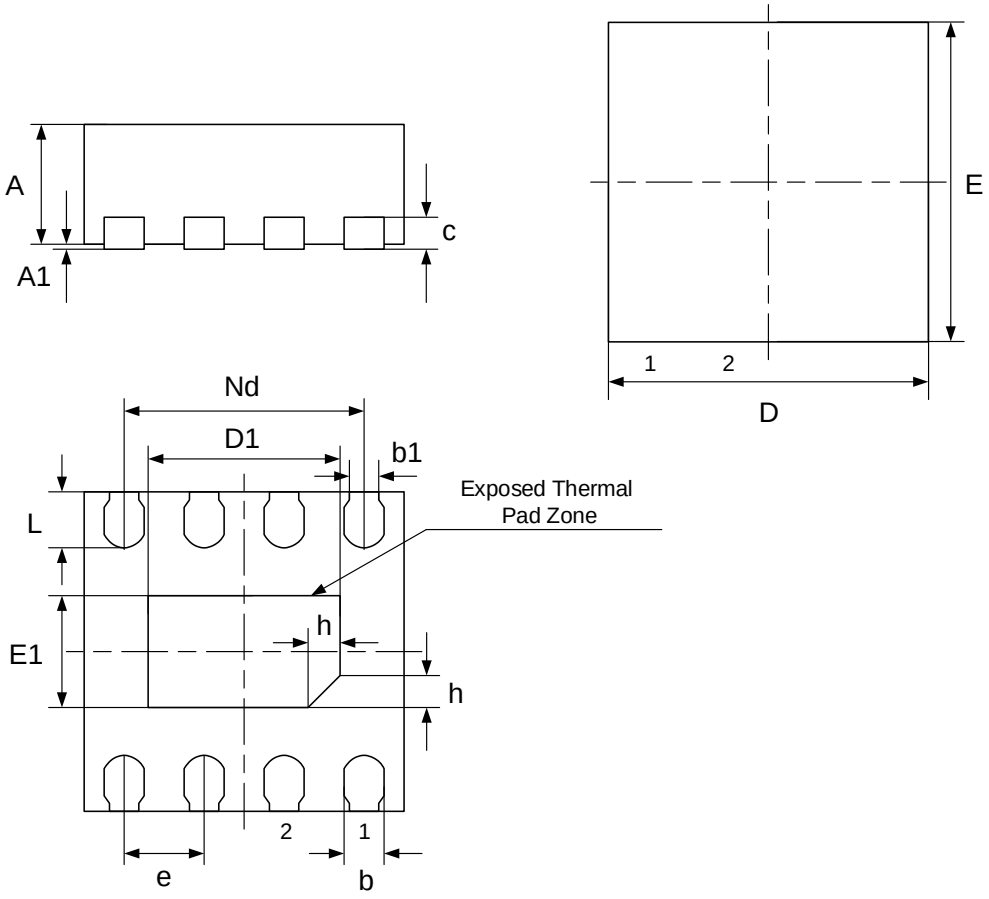
NOTES: (continued)

1. Refer to the Table 3 *SC70-5L dimensions(mm)*.

Table 3. SC70-5L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.90		1.10
A1	0.00		0.10
A2	0.90		1.00
b	0.15		0.35
c	0.08		0.15
D	2.00		2.20
E	2.15		2.45
E1	1.15		1.35
e	0.65 BSC		
e1	1.30 BSC		
L	0.525 REF		
L1	0.26		0.46
θ	0°		8°

DFN2x2-8L Package Outline



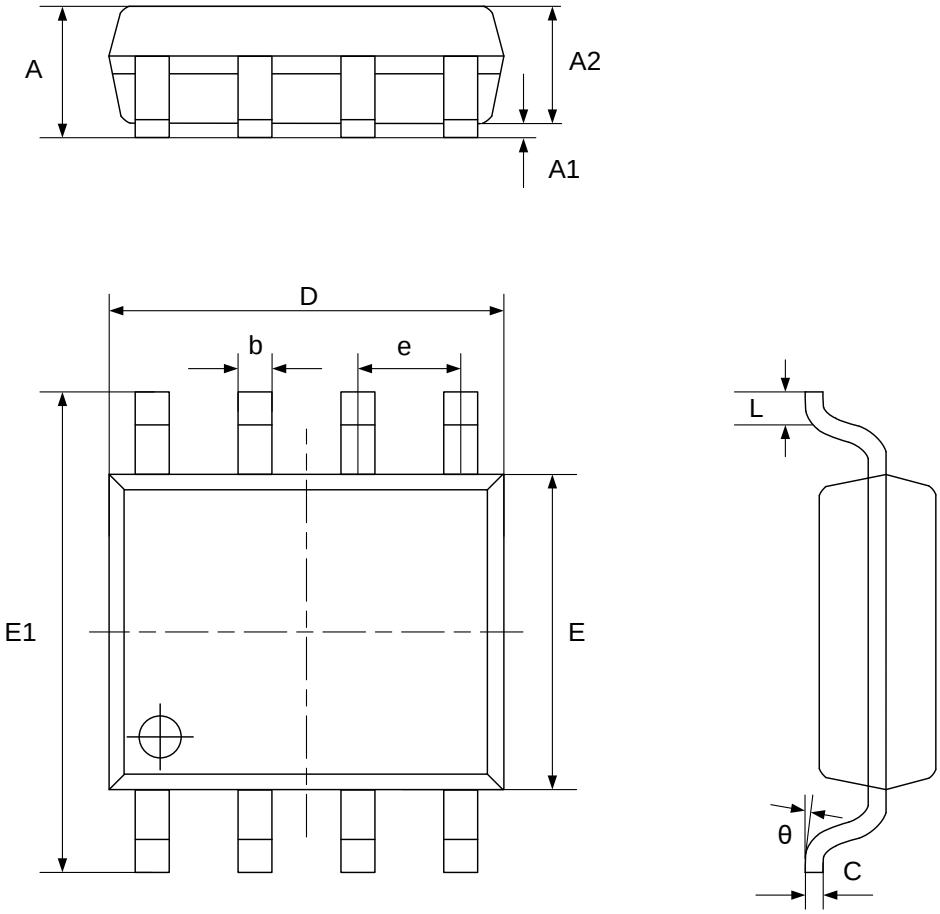
NOTES: (continued)

1. Refer to the Table 4 *DFN2x2-8L dimensions(mm)*.

Table 4. DFN2x2-8L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c	0.18	0.20	0.25
D	1.90	2.00	1.30
D1	1.10	1.20	1.30
Nd		1.50 BSC	
E	1.90	2.00	2.10
E1	0.60	0.70	0.80
e		0.50 BSC	
L	0.30	0.35	0.40
h	0.15	0.20	0.25

SOIC-8L Package Outline



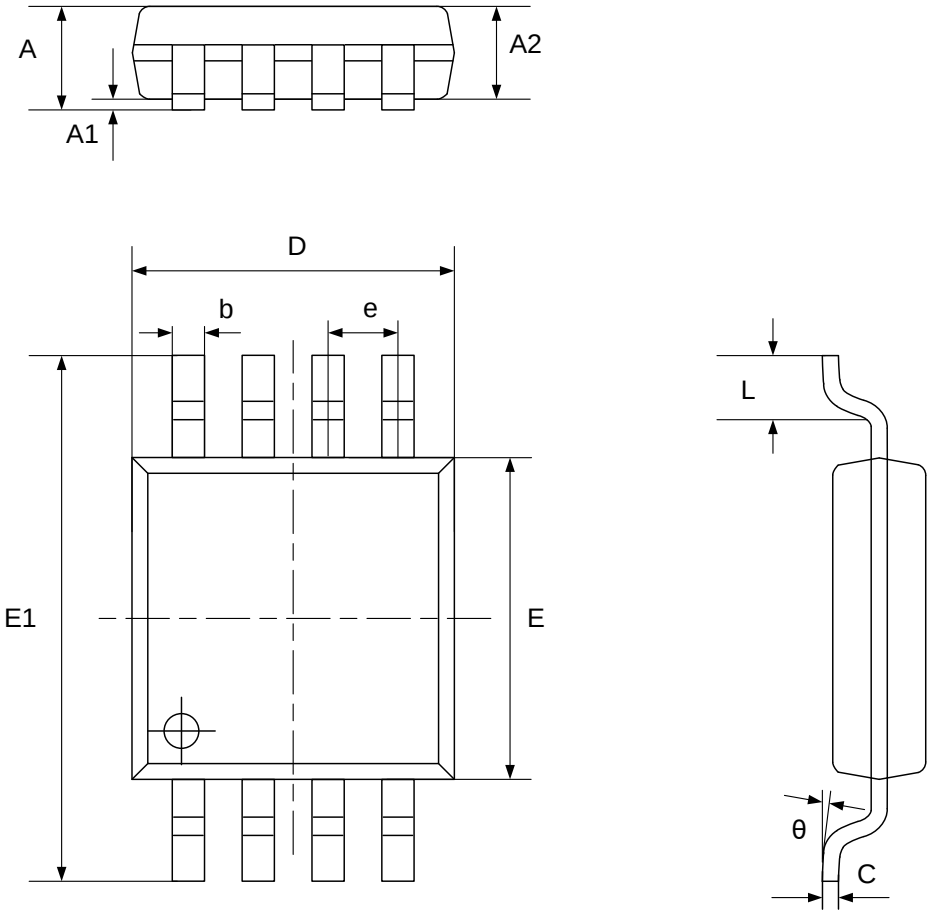
NOTES: (continued)

1. Refer to the Table 5 *SOIC-8L dimensions(mm)*.

Table 5. SOIC-8L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	1.370		1.670
A1	0.070		0.170
A2	1.300		1.500
b	0.306		0.506
C		0.203	
D	4.700		5.100
E	3.820		4.020
E1	5.800		6.200
e		1.270	
L	0.450		0.750
θ	0°		8°

MSOP-8L Package Outline



NOTES: (continued)

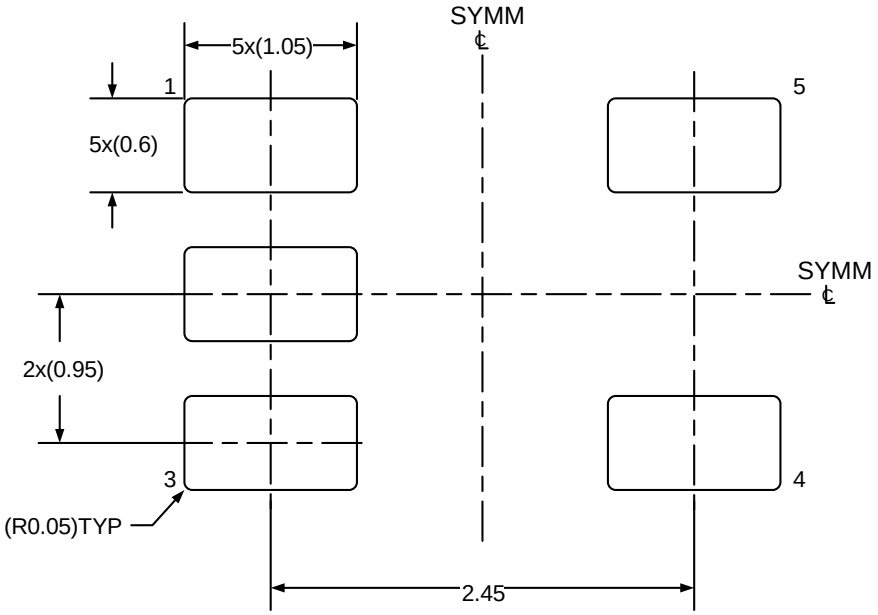
1. Refer to the Table 6 *MSOP-8L dimensions(mm)*.

Table 6. MSOP-8L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.800		1.100
A1	0.050		0.150
A2	0.750		0.950
b	0.290		0.380
C	0.150		0.200
D	2.900		3.100
E	2.900		3.100
E1	4.700		5.100
e		0.650	
L	0.400		0.700
θ	0°		8°

8.2 Recommended Land Pattern

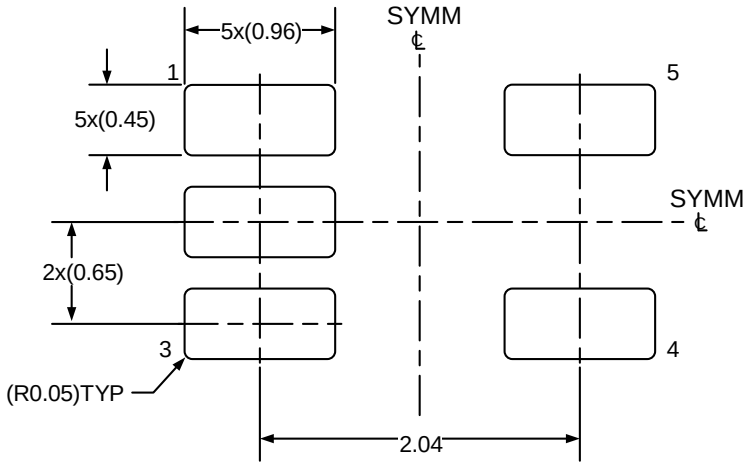
SOT23-5 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

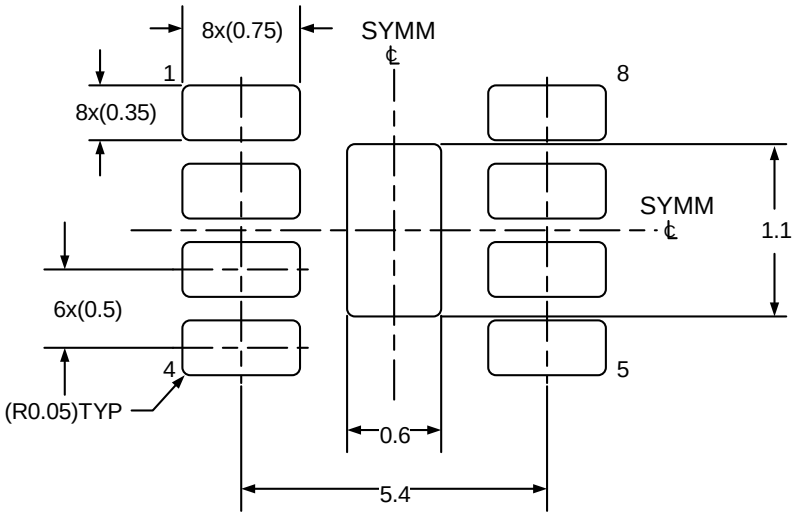
SC70-5L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

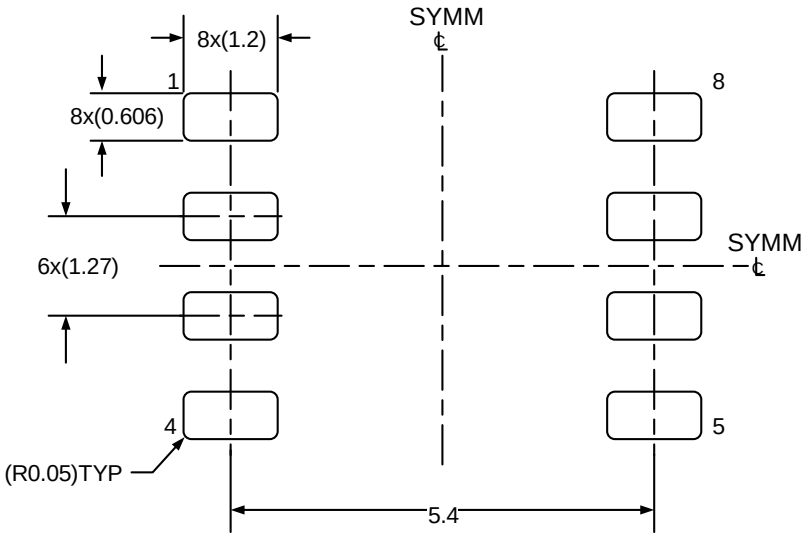
DFN2x2-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

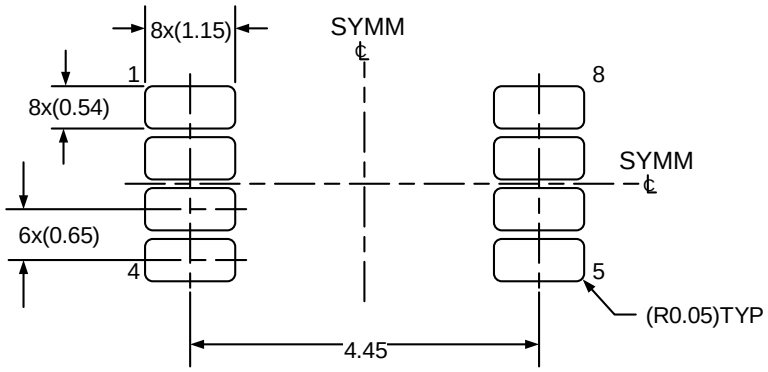
SOIC-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

MSOP-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30AP8551NSTR-I01	SOT23-5L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP8551WLTR-I01	SOIC-8L	Green	Tape & Reel	4000	−40°C to +125°C
GD30AP8552WETR-I02	DFN2x2-8L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP8552WLTR-I02	SOIC-8L	Green	Tape & Reel	4000	−40°C to +125°C
GD30AP8552WMTR-I02	MSOP-8L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP8553NSTR-I01	SOT23-5L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP8553NDTR-I01	SC70-5L	Green	Tape & Reel	3000	−40°C to +125°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

Important Notice

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