General Purpose 1.2MHz, RRIO, 1.8V CMOS Amplifiers

1 Features

- General Purpose Amplifiers for Cost-Sensitive Systems
- 1.2MHz GBW for Unity-Gain Stable
- Micro-Power: 85μA Supply Current Per Amplifier
- Low Input Offset Voltage: ±3.0mV Maximum
- Low Noise: 30nV/√Hz at 1kHz
- Single 1.8V to 5.5V Supply Voltage Range
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Extended Temperature Range: −40°C to +125°C

2 Applications

- Battery-Powered Instruments:
  - Consumer, Industrial, Medical, Notebooks
- Audio Outputs
- Wireless Sensors:
  - Home Security, Remote Sensing, Wireless Metering
- Sensor Signal Conditioning:
  - Sensor Interfaces, Loop-Powered, Active Filters

3 Description

The GD30AP321/GD30AP358/GD30AP324 family of single-, dual-, and quad- channel operational amplifiers is specifically designed for general-purpose cost-sensitive systems and applications. Featuring rail-to-rail input and output(RRIO) swings, and low quiescent current(typical 85μA) combined with a wide bandwidth(1.2MHz) and low noise(30nV/√Hz at 1 kHz) makes this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance, such as audio outputs, consumer electronics, smoke detectors, portable medical devices and white goods. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the GD30AP321/GD30AP358/GD30AP324 family provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 500pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge(ESD) protection(5kV HBM). The GD30AP321/GD30AP358/GD30AP324 amplifiers are optimized for operation at voltages as low as +1.8V (±0.9V) and up to +5.5V (±2.75V), and over the extended temperature range of −40°C to +125°C.

GD30AP321(single) is available in both SOT23-5L and SC70-5L packages. The GD30AP358(dual) is offered in SOIC-8L, DFN2X2-8L, MSOP-8L packages. The qual-channel GD30AP324 is offered in SOIC-14L, TSSOP-14L, QFN3X3-16L packages.

Device Information[1]

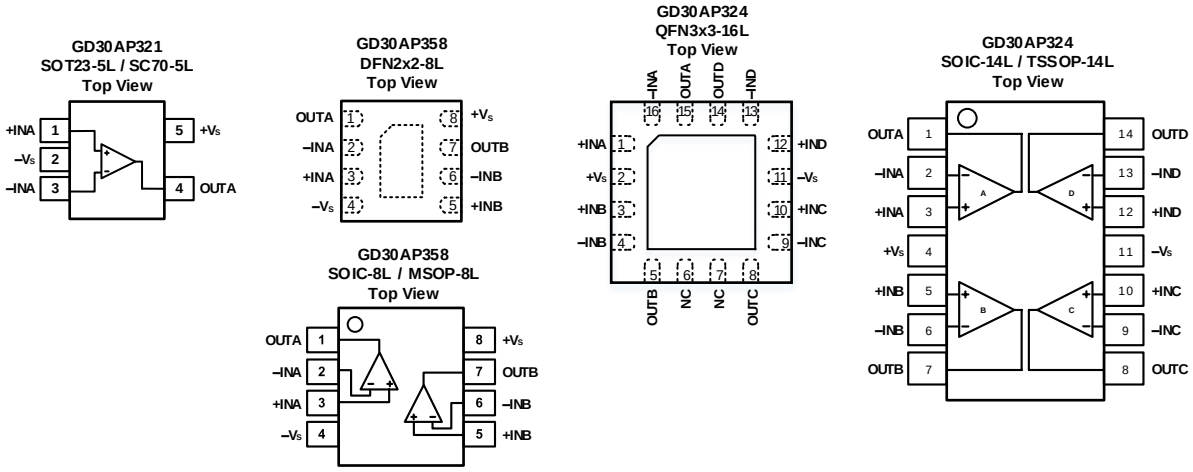
PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30AP321	SOT23-5L	2.92mm x 1.63mm
	SC70-5L	2.10mm x 1.25mm
GD30AP358	DFN2x2-8L	2.00mm x 2.00mm
	SOIC-8L	4.90mm x 3.92mm
	MSOP-8L	3.00mm x 3.00mm
GD30AP324	QFN3x3-16L	3.00mm x 3.00mm
	SOIC-14L	8.73mm x 3.95mm
	TSSOP-14L	4.96mm x 4.40mm

1. For all available packages, see the *Package Information* and *Ordering Information* at the end of data sheet.

Table of Contents

4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

NAME	PIN TYPE[1]	FUNCTION
-IN	I	Inverting input of the amplifier. The voltage range is from (V_{S-} − 0.1V) to (V_{S+} + 0.1V).
+IN	I	Non-inverting input of the amplifier. This pin has the same voltage range as –IN.
$+V_S$	P	Positive power supply.
$-V_S$	P	Negative power supply.
OUT	O	Amplifier output.

1. I = Input, O = Output, P = Power.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{S+} to V_{S-}	Supply voltage		10	V
V_I	Signal input voltage	V_{S-} − 0.5	V_{S+} + 0.5	V
I_I	Signal input current	−10	10	mA
	Duration of output short circuit		Continuous	s
T_J	Operating junction temperature		150	°C
T_{stg}	Storage temperature	−65	150	°C
	Lead Temperature Range (Soldering 10 sec)		260	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.
2. Differential voltages are at IN+, with respect to IN-.
3. Short circuits from outputs to V_S can cause excessive heating and eventual destruction.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{S-} to V_{S+}	Input supply voltage range	1.8		5.5	V
V_{CM}	Common-mode voltage range	V_{S-} − 0.1		V_{S+} + 0.1	V
T_A	Operating temperature range	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±5000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±2000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	SC70-5L	333	°C/W
		SOT23-5L	190	
		DFN2x2-8L	94	
		MSOP-8L	201	
		SOIC-8L	125	

Thermal Resistance(continued)

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	QFN3x3-16L	65	°C/W
		TSSOP-14L	112	
		SOIC-14L	115	

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_S = 5.0V, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, T_A = +25°C, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±0.7	±3.0	mV
dV_{OS}/d_T	Input offset voltage drift[1]	T_A = −40°C to 125°C		±1	3.5	µV/°C
PSRR	Power supply rejection ratio	V_S = 2.0 to 5.5V, V_{CM} < V_{S+} − 2V	80	110		dB
		T_A = −40 to +125°C	75			
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		V_{S+} − 0.1		V_{S+} + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5V, V_{CM} = −0.1 to 5.6V	70	83		dB
		V_{CM} = 0 to 5.3V, T_A = −40 to +125°C	65			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.1V	65	77		
		V_{CM} = 0 to 1.8V, T_A = −40 to +125°C	60			
INPUT BIAS CURRENT						
I_B	Input bias current[1]			5	50	pA
		T_A = −40°C to 85°C			200	
		T_A = −40°C to 125°C			2000	
I_{OS}	Input offset current[1]			10	50	pA
NOISE						
V_n	Input voltage noise	f = 0.1 to 10Hz		6		μV_{P-P}
e_n	Input voltage noise density	f = 10kHz		27		nV/√Hz
		f = 1kHz		30		
I_n	Input current noise density	f = 1kHz		5		fA/√Hz
INPUT IMPEDANCE						
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	R_L = 50kΩ, V_O = 0.05 to 3.5V	90	105		dB

Electrical Characteristics(continued)

V_S = 5.0V, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, T_A = +25°C, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
		T_A = −40°C to 125°C	85			
		R_L = 2kΩ, V_O = 0.15 to 3.5V	85	100		
		T_A = −40°C to 125°C	80			
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1.2		MHz
SR	Slew rate	G = +1, C_L = 100pF, V_O = 1.5 to 3.5V		1		V/μs
THD+N	Total harmonic distortion + noise	G = +1, f = 1kHz, V_O = $1V_{RMS}$		0.003		%
t_S	Settling time	To 0.1%, G = +1, 1V step		1.5		μs
		To 0.01%, G = +1, 1V step		1.8		
t_{OR}	Overdrive recovery time	To 0.1%, VIN * Gain > V_S		2.5		μs
OUTPUT						
V_{OH}	High output voltage swing	R_L = 50kΩ	V_{S+} − 6	V_{S+} − 3		mV
		R_L = 2kΩ	V_{S+} − 100	V_{S+} − 65		
V_{OL}	Low output voltage swing	R_L = 50kΩ		V_{S-} + 2	V_{S-} + 4	mV
		R_L = 2kΩ		V_{S-} + 42	V_{S-} + 65	
I_{SC}	Short-circuit current	Source current through 10Ω		40		mA
		Sink current through 10Ω		50		
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)			85	120	μA
		T_A = −40 to +125°C			150	

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, at T_A = +25°C, unless otherwise noted.

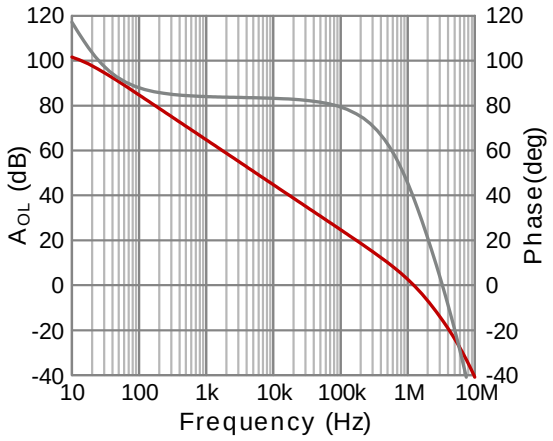


Figure 1. Open-loop Gain and Phase vs. Frequency

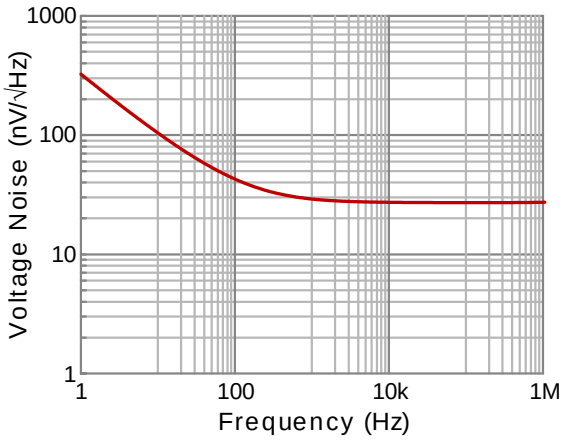


Figure 2. Input Voltage Noise Spectral Density vs. Frequency

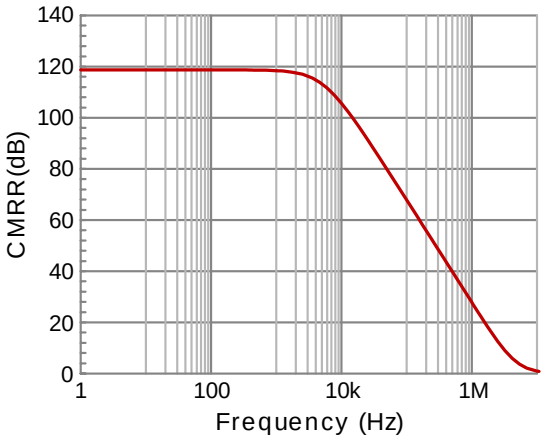


Figure 3. Common Mode Rejection Ratio vs. Frequency

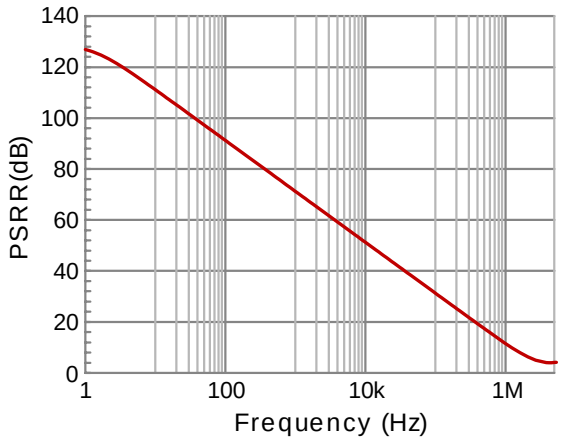


Figure 4. Power Supply Rejection Ratio vs. Frequency

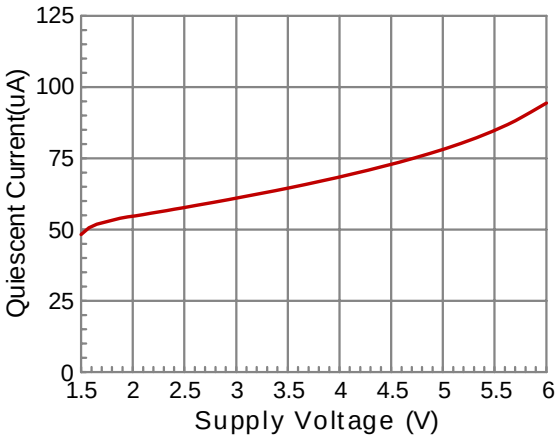


Figure 5. Quiescent Current vs. Supply Voltage

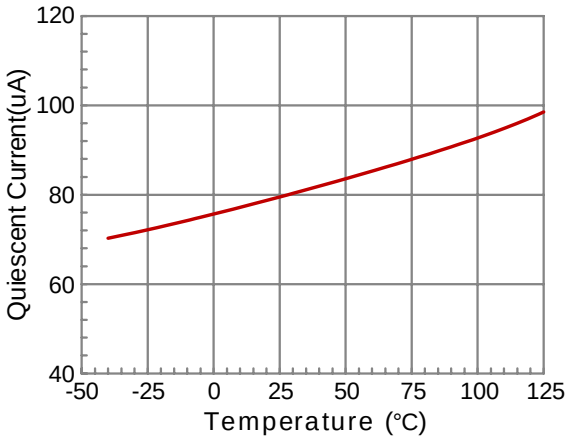


Figure 6. Quiescent Current vs. Temperature

Typical Characteristics(continued)

V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, at T_A = +25°C, unless otherwise noted.

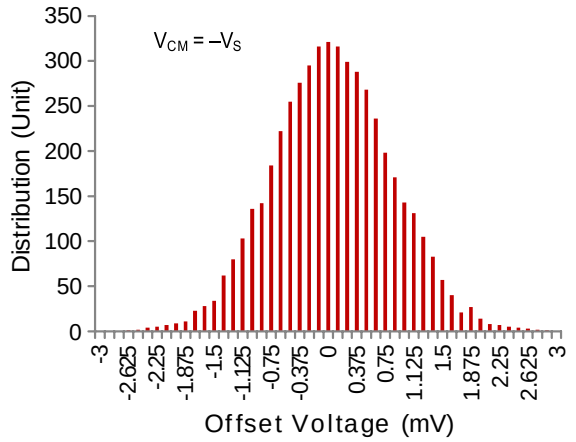


Figure 7. Offset Voltage Production Distribution

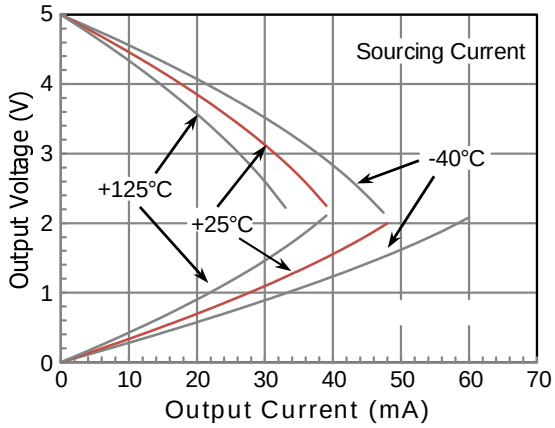


Figure 8. Output Voltage Swing vs. Output Current

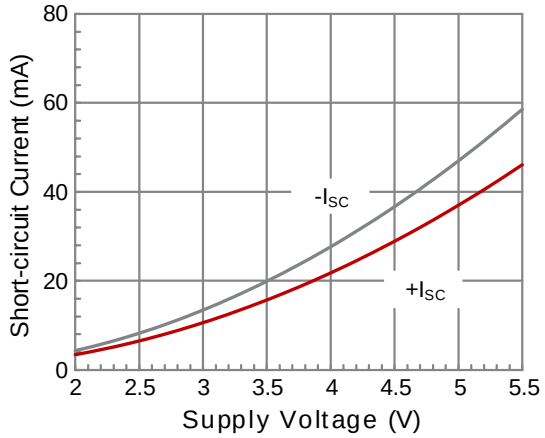


Figure 9. Short-circuit Current vs. Supply Voltage

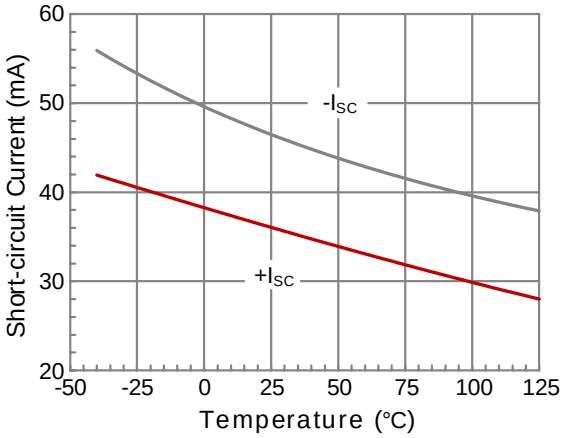


Figure 10. Short-circuit Current vs. Temperature

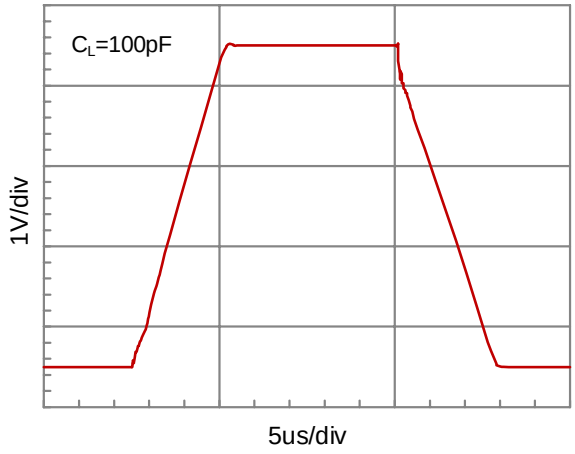


Figure 11. Large Signal Step Response

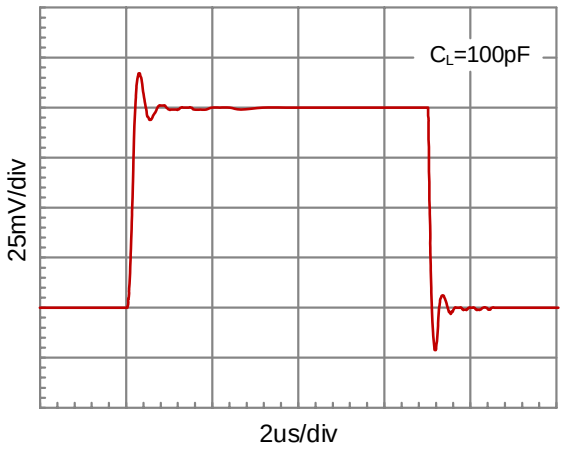


Figure 12. Small Signal Step Response

6 Functional Description

The GD30AP321/GD30AP358/GD30AP324 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8V to 5.5V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤10kΩ loads connected to any point between V_{S+} and ground. The input common-mode voltage range includes both rails, and allows the GD30AP321/GD30AP358/GD30AP324 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters(ADCs).

The GD30AP321/GD30AP358/GD30AP324 features 1.2MHz bandwidth and 1V/μs slew rate with only 85μA supply current per amplifier, providing good ac performance at very low power consumption. DC applications are also well served with a low input noise voltage of 30nV/√Hz at 1kHz, low input bias current, and an input offset voltage of ±3.0mV maximum. The typical offset voltage drift is 1μV/°C, over the full temperature range the input offset voltage changes only 100μV(0.7mV to 0.8mV).

6.1 Operating Voltage

The GD30AP321/GD30AP358/GD30AP324 family is optimized for operation at voltages as low as +1.8V(±0.9V) and up to +5.5V(±2.75V). In addition, many specifications apply from −40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages(V_{S+} to V_{S-}) higher than +10V can permanently damage the device.

6.2 Rail-To-Rail Input

The input common-mode voltage range of the GD30AP321/GD30AP358/GD30AP324 extends 100mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}−1.4V to the positive supply, whereas the P-channel pair is active for inputs from 100mV below the negative supply to approximately V_{S+}–1.4V. There is a small transition region, typically V_{S+}−1.2V to V_{S+}−1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region(both stages on) can range from V_{S+}−1.4V to V_{S+}−1.2V on the low end, up to V_{S+}−1V to V_{S+}−0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the GD30AP321/GD30AP358/GD30AP324 during normal operation is approximately 5pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference(EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

6.3 Input EMI Filter And Clamp Circuit

Figure 13 shows the input EMI filter and clamp circuit. The GD30AP321/GD30AP358/GD30AP324 op-amps have internal ESD protection diodes(D1, D2, D3, and D4) that are connected between the inputs and each supply rail.

These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 20mA as stated in the Absolute Maximum Ratings.

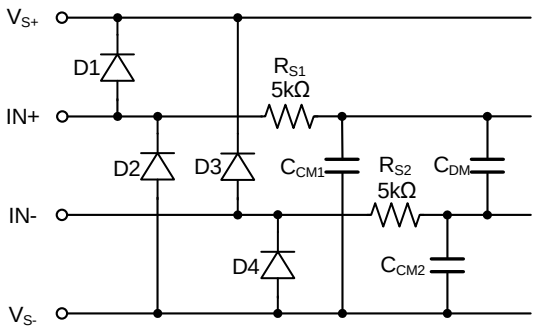


Figure 13. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the DC offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the GD30AP321/GD30AP358/GD30AP324 is composed of two 5kΩ input series resistors(R_{S1} and R_{S2}), two common-mode capacitors(C_{CM1} and C_{CM2}), and a differential capacitor(C_{DM}). These RC networks set the −3dB low-pass cutoff frequencies at 35MHz for common-mode signals, and at 22MHz for differential signals.

6.4 Rail-To-Rail Output

Designed as a micro-power, low-noise op-amp, the GD30AP321/GD30AP358/GD30AP324 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 50kΩ, the output swings typically to within 3mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 2kΩ, the output swings typically to within 65mV of the positive supply rail and within 42mV of the negative supply rail.

6.5 Capacitive Load And Stability

The GD30AP321/GD30AP358/GD30AP324 family can safely drive capacitive loads of up to 500pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if these op-amps must drive a load exceeding 500pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 14. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

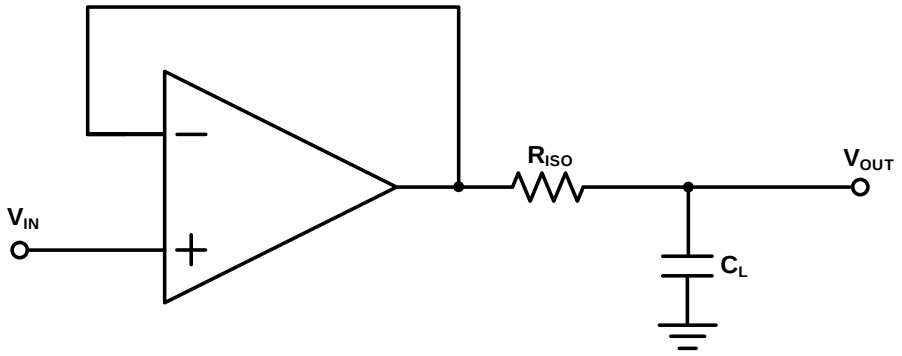


Figure 14. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 15. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

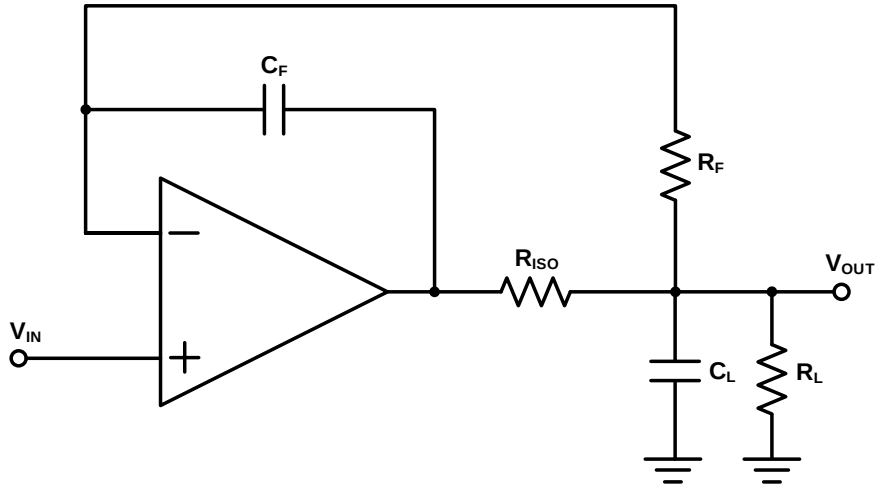


Figure 15. Indirectly Driving Heavy Capacitive Load with DC Accuracy

6.6 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the GD30AP321/GD30AP358/GD30AP324 is approximately 2.5μs.

6.7 EMI Rejection Ratio

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins —— the non-inverting input, inverting input, positive supply, negative supply, and output pins are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board(PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or R_F signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a DC offset at the output.

The GD30AP321/GD30AP358/GD30AP324 have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\log(VIN_{IN\_PEAK}/\Delta V_{OS}) \quad (1)$$

6.8 Input-To-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

6.9 Maximizing Performance Through Proper Layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the GD30AP321/GD30AP358/GD30AP324, care is needed in layout the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 16 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

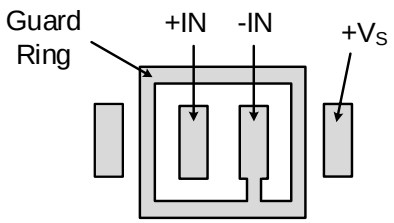


Figure 16. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at

the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

7 Application Information

7.1 Typical Application

The GD30AP321/GD30AP358/GD30AP324 amplifiers can be widely used in various signal conditioning applications. One of typical application for operational amplifier is an inverting amplifier. Application in Figure 17 reverses the input voltage and the magnitude of voltage is amplified, reduced or maintained according to a certain proportion.

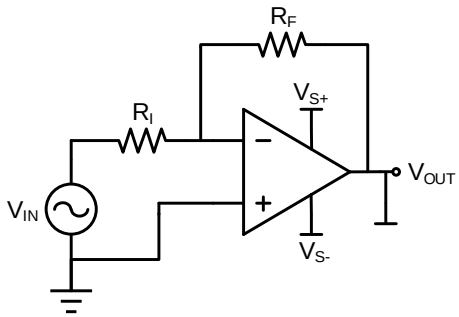


Figure 17. Application Schematic

7.2 Function Description

This application requires the function of voltage amplification, which need to scales a signal of ±0.5V to ±1.8V.The supply voltage of amplifiers must be chosen large than the input voltage range and output voltage range. At the same time, The amplifiers is power by a dual power supply because the input voltage is an AC signal.

7.3 Detailed Design

Determine the gain required of the inverting amplifier by Equation(2):

$$A_V = \frac{VOUT}{VIN} = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

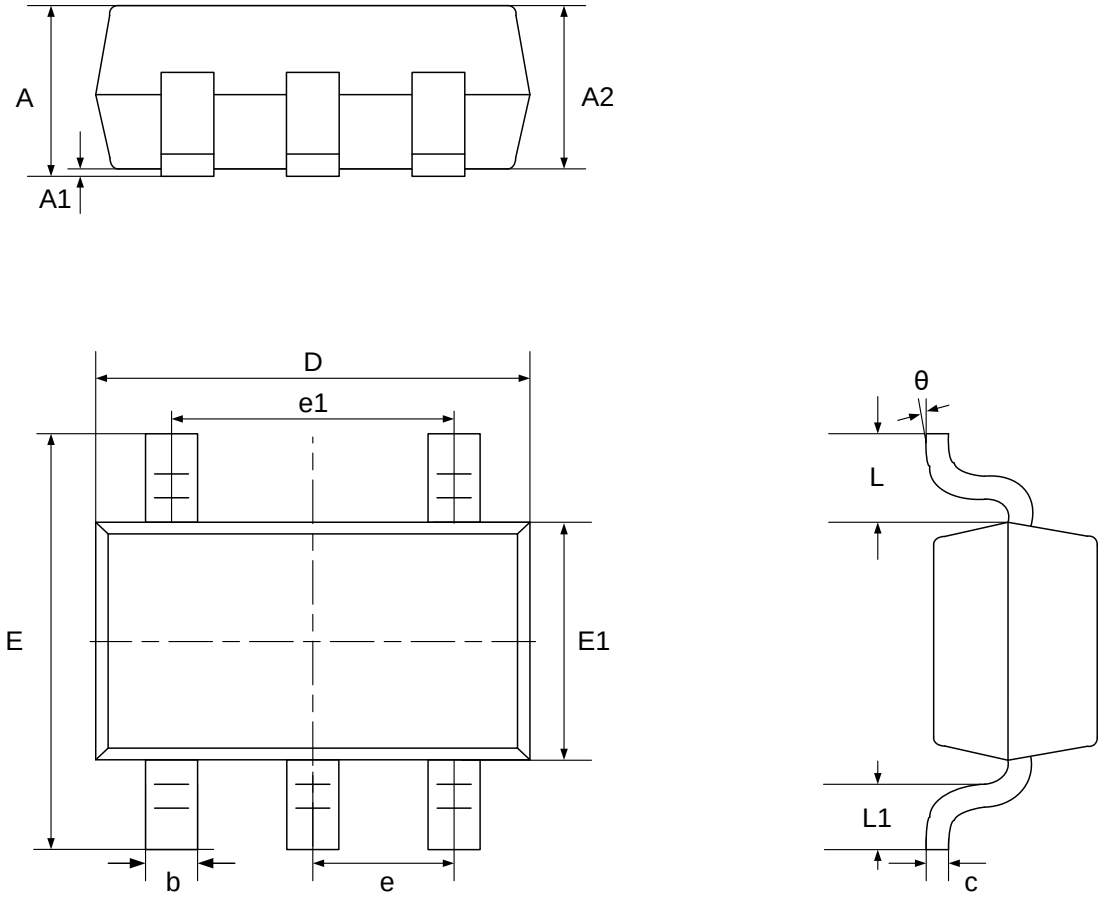
Because the transfer function of inverting amplifier is highly reliant on resistors(R_I、R_F), used resistors with low tolerances to maximize performance and minimize error. The current of amplifiers circuit is in milliampere range. So the value of resistors need to keep in the kilohm range at least. The value of 10kΩ for R_I and 36kΩ for R_F is suitable in this application. The voltage conversion coefficient of inverting amplifier was determined by Equation(3):

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

8 Package Information

8.1 Outline Dimensions

SOT23-5L Package Outline



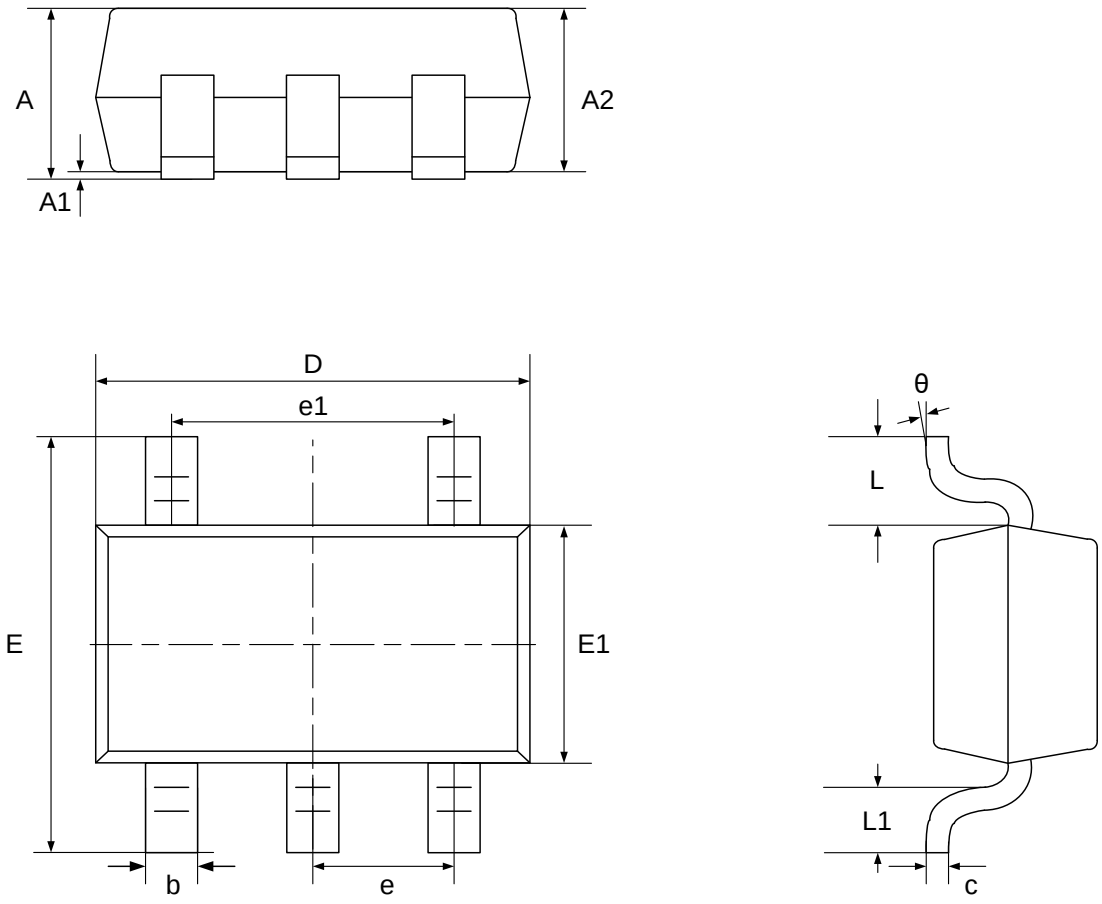
NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 1 *SOT23-5L dimensions(mm)*.

Table 1. SOT23-5L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A			1.35
A1	0.00		0.15
A2	1.00		1.20
b	0.35		0.45
c	0.14		0.20
D	2.82		3.02
E	2.60		3.00
E1	1.526		1.726
e	0.95 BSC		
e1	1.90 BSC		
L	0.60 REF		
L1	0.30		0.60
θ	0°		8°

SC70-5L Package Outline



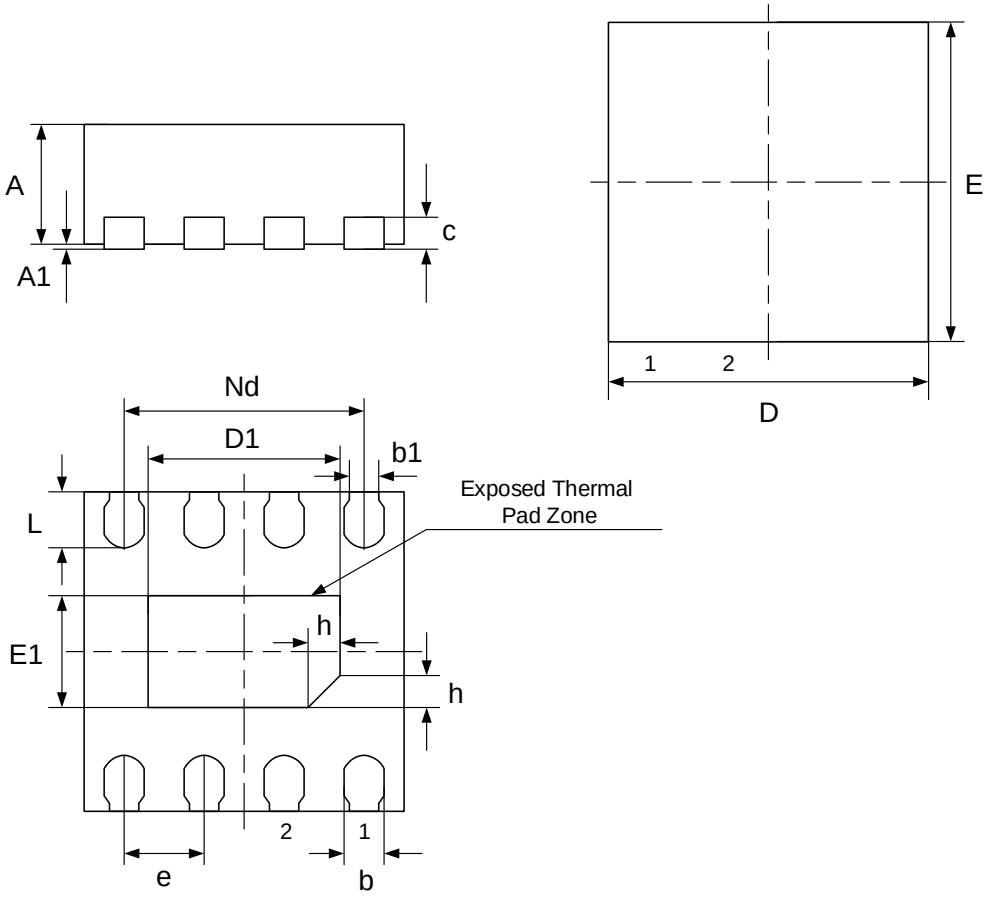
NOTES: (continued)

1. Refer to the Table 2 *SC70-5L dimensions(mm)*.

Table 2. SC70-5L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.90		1.10
A1	0.00		0.10
A2	0.90		1.00
b	0.15		0.35
c	0.08		0.15
D	2.00		2.20
E	2.15		2.45
E1	1.15		1.35
e	0.65 BSC		
e1	1.30 BSC		
L	0.525 REF		
L1	0.26		0.46
θ	0°		8°

DFN2x2-8L Package Outline



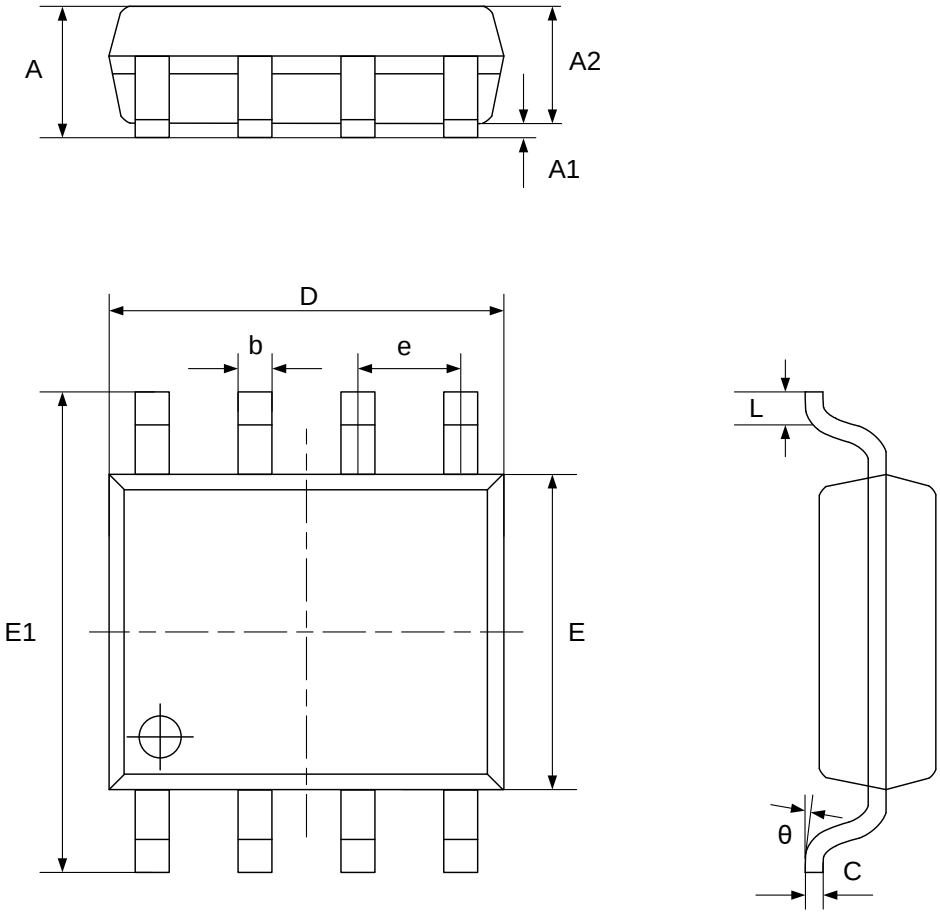
NOTES: (continued)

1. Refer to the Table 3 *DFN2x2-8L dimensions(mm)*.

Table 3. DFN2x2-8L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.20	0.25	0.30
b1		0.18 REF	
c	0.18	0.20	0.25
D	1.90	2.00	1.30
D1	1.10	1.20	1.30
Nd		1.50 BSC	
E	1.90	2.00	2.10
E1	0.60	0.70	0.80
e		0.50 BSC	
L	0.30	0.35	0.40
h	0.15	0.20	0.25

SOIC-8L Package Outline



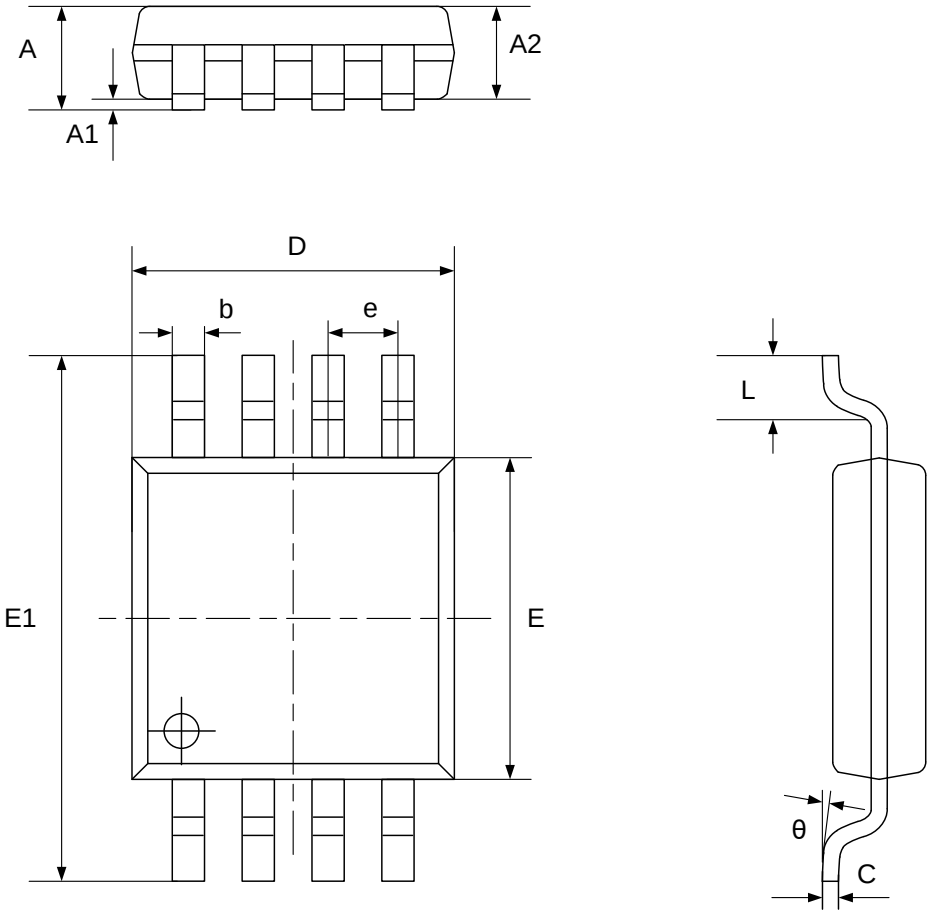
NOTES: (continued)

1. Refer to the Table 4 *SOIC-8L dimensions(mm)*.

Table 4. SOIC-8L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	1.370		1.670
A1	0.070		0.170
A2	1.300		1.500
b	0.306		0.506
C		0.203	
D	4.700		5.100
E	3.820		4.020
E1	5.800		6.200
e		1.270	
L	0.450		0.750
θ	0°		8°

MSOP-8L Package Outline



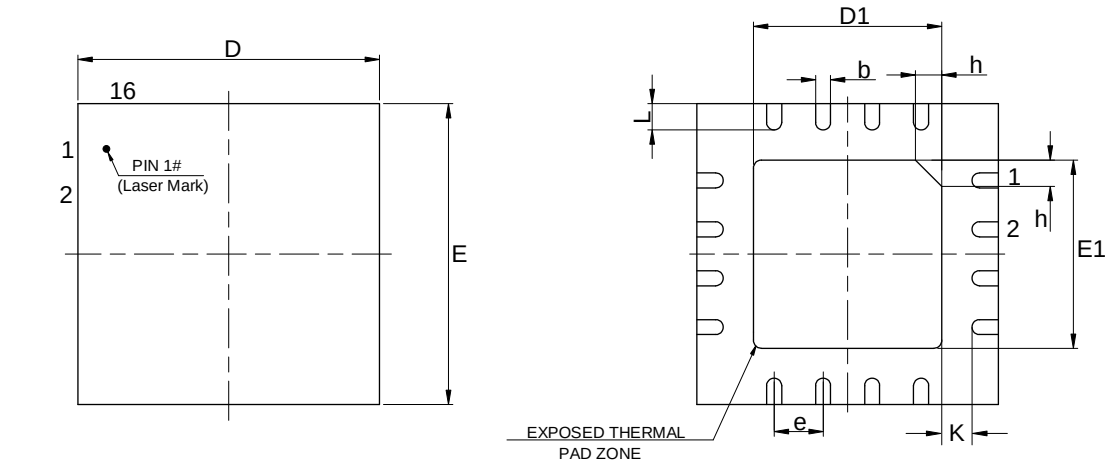
NOTES: (continued)

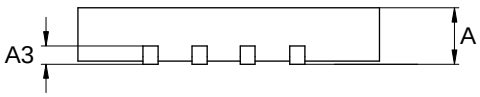
1. Refer to the Table 5 *MSOP-8L dimensions(mm)*.

Table 5. MSOP-8L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.800		1.100
A1	0.050		0.150
A2	0.750		0.950
b	0.290		0.380
C	0.150		0.200
D	2.900		3.100
E	2.900		3.100
E1	4.700		5.100
e		0.650	
L	0.400		0.700
θ	0°		8°

QFN3x3-16L Package Outline





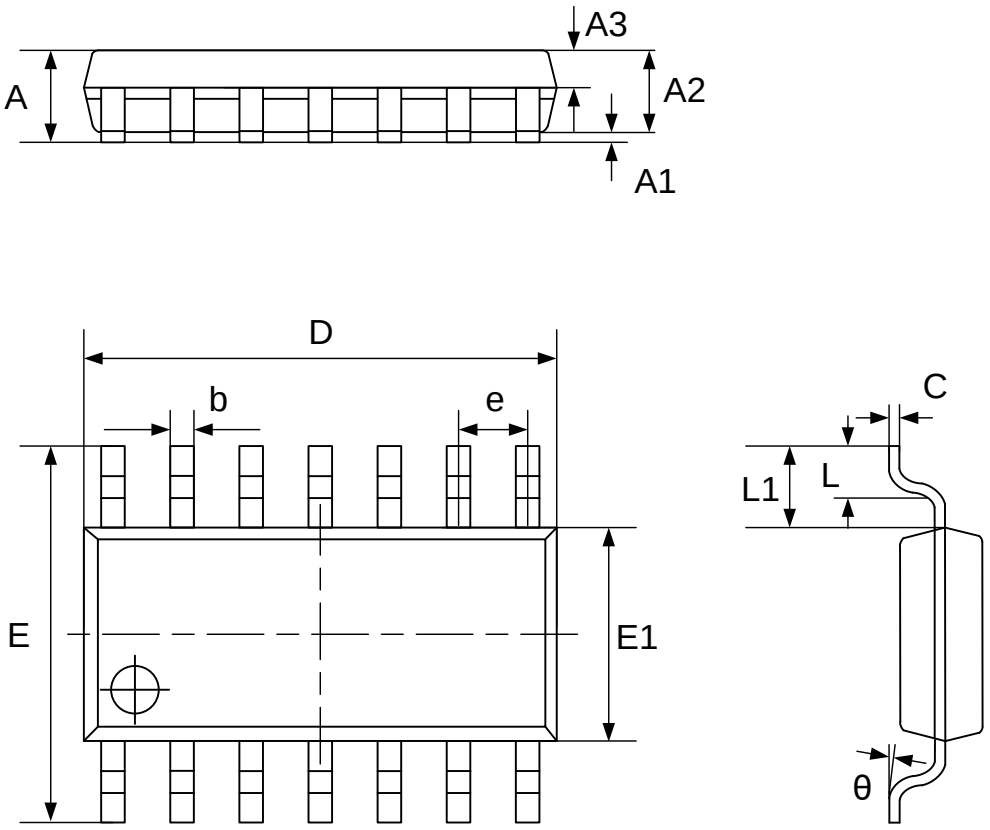
NOTES: (continued)

1. Refer to the Table 6 *QFN3x3-16L dimensions(mm)*.

Table 6. QFN3x3-16L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A3		0.210 REF	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D1	1.60	1.65	1.70
E	2.90	3.00	3.10
E1	1.60	1.65	1.70
e		0.50 BSC	
h	0.20	0.25	0.30
K	0.225	0.275	0.325
L	0.35	0.40	0.45

SOIC-14L Package Outline



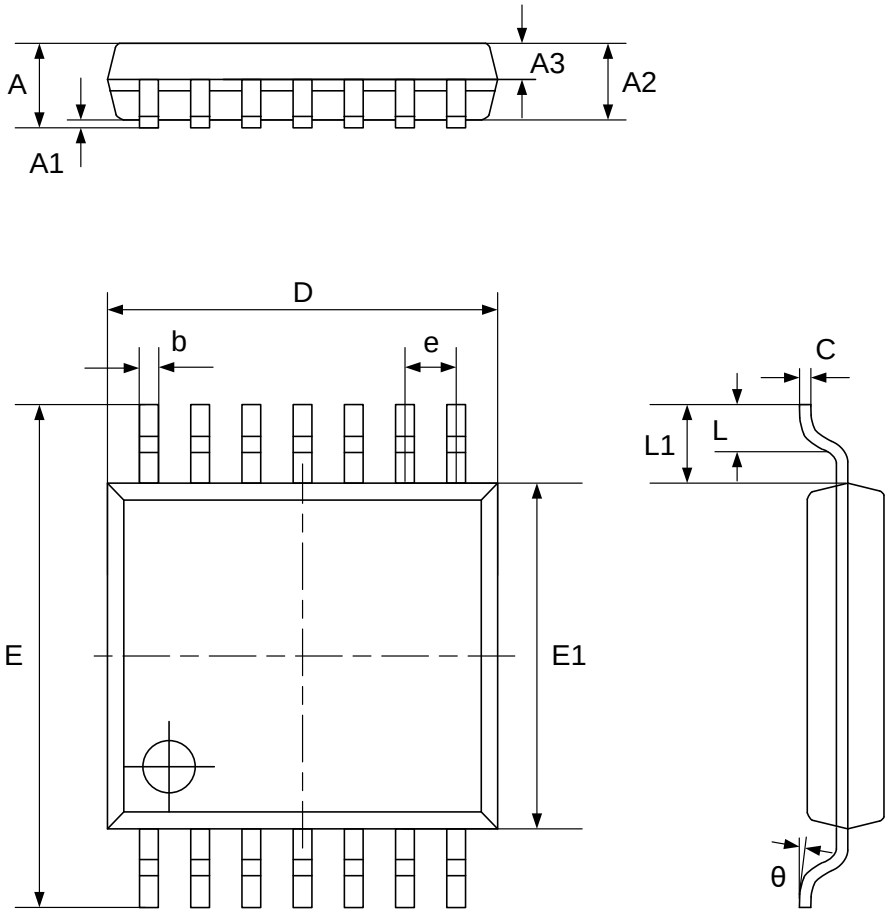
NOTES: (continued)

1. Refer to the Table 7 *SOIC-14L dimensions(mm)*.

Table 7. SOIC-14L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	1.450		1.850
A1	0.100		0.300
A2	1.350		1.550
A3	0.550		0.750
b		0.406	
C		0.203	
D	8.630		8.830
E	5.840		6.240
E1	3.850		4.050
e		1.270	
L1	1.040 REF		
L	0.350		0.750
θ	2°		8°

TSSOP-14L Package Outline



NOTES: (continued)

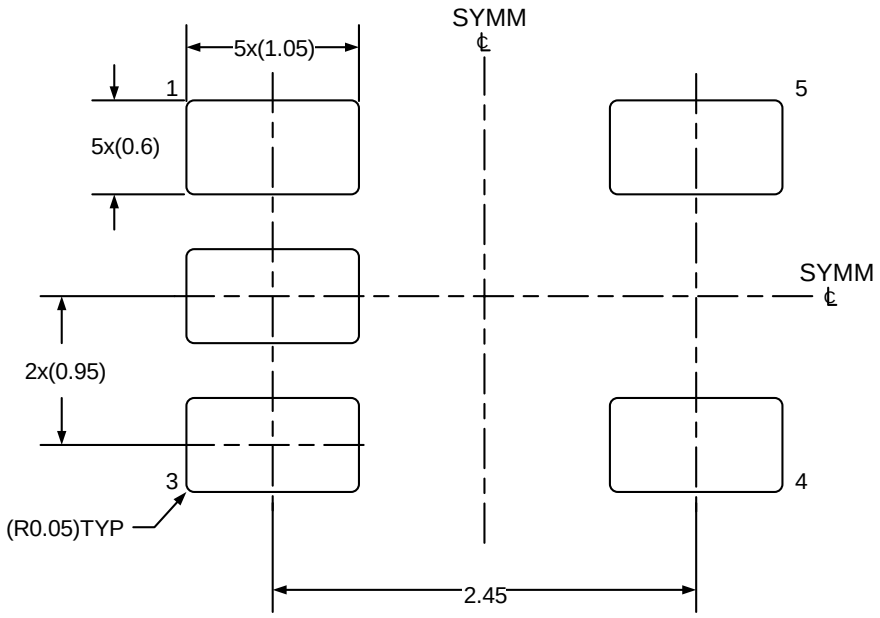
1. Refer to the Table 8 *TSSOP-14L dimensions(mm).*

Table 8. TSSOP-14L dimensions(mm)

SYMBOL	MIN	TYP	MAX
A			1.200
A1	0.050		0.150
A2	0.900		1.050
A3	0.390		0.490
b	0.200		0.290
C	0.130		0.180
D	4.860		5.060
E	6.200		6.600
E1	4.300		4.500
e		0.650	
L1	1.000 REF		
L	0.450		0.750
θ	0°		8°

8.2 Recommended Land Pattern

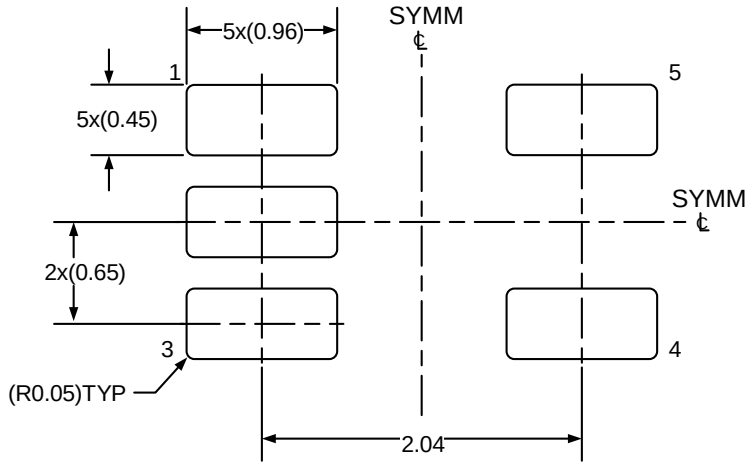
SOT23-5L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

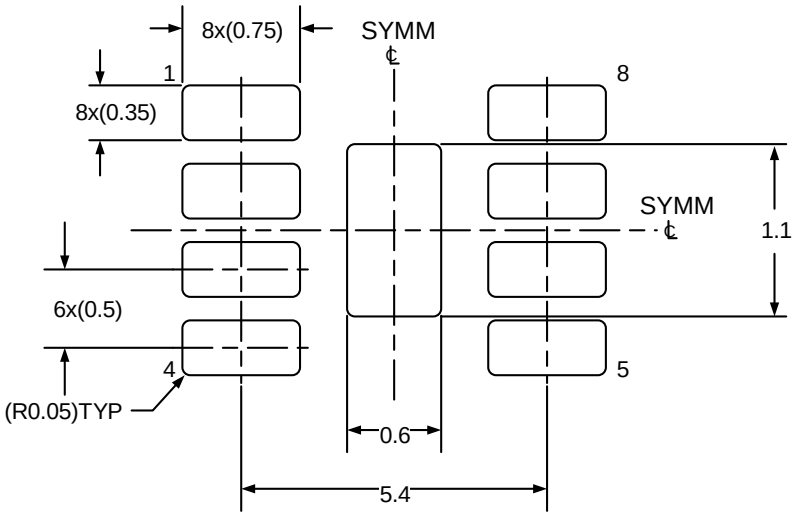
SC70-5L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

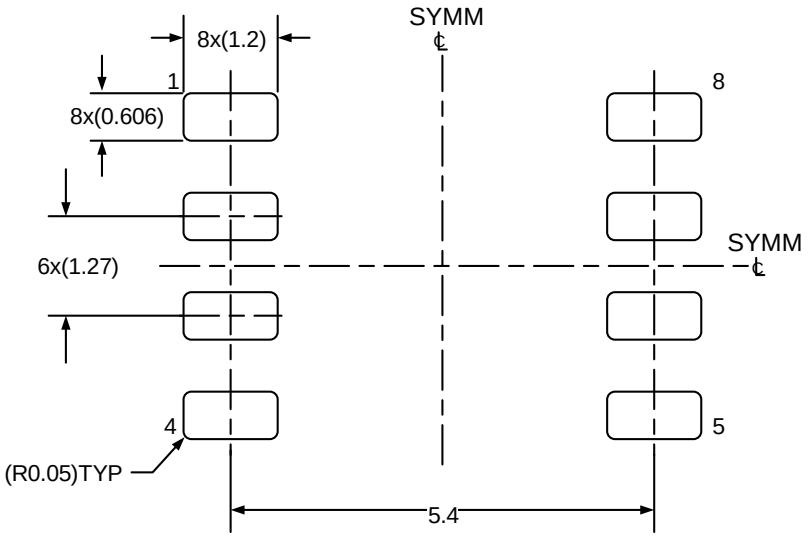
DFN2x2-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

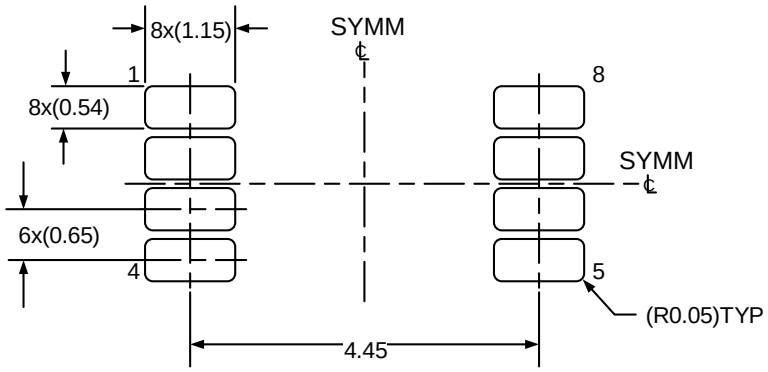
SOIC-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

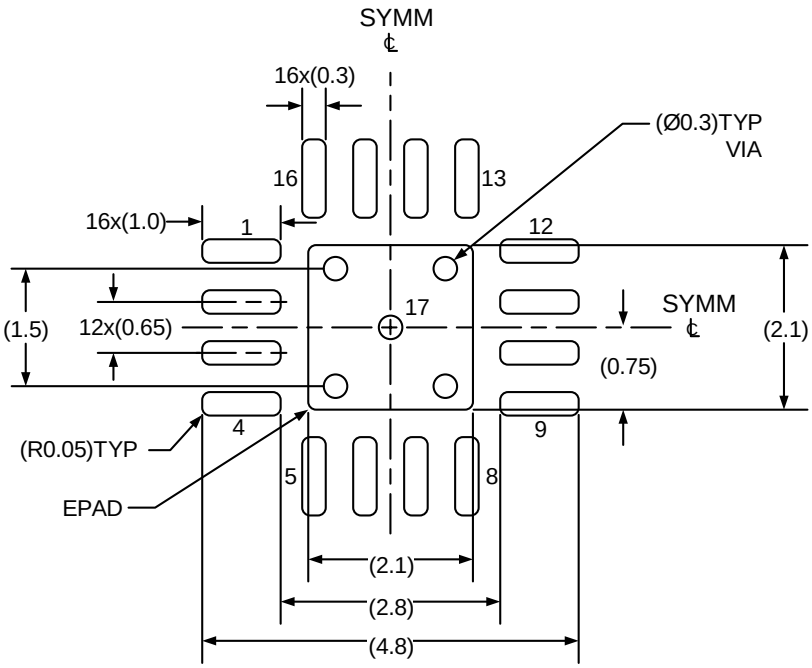
MSOP-8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

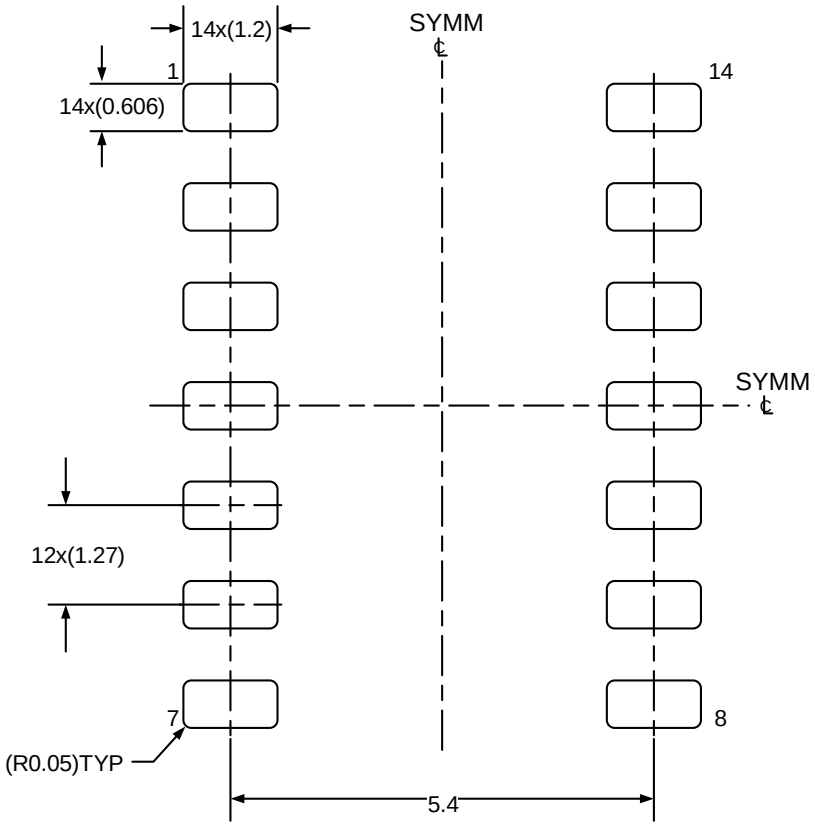
QFN3x3-16L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

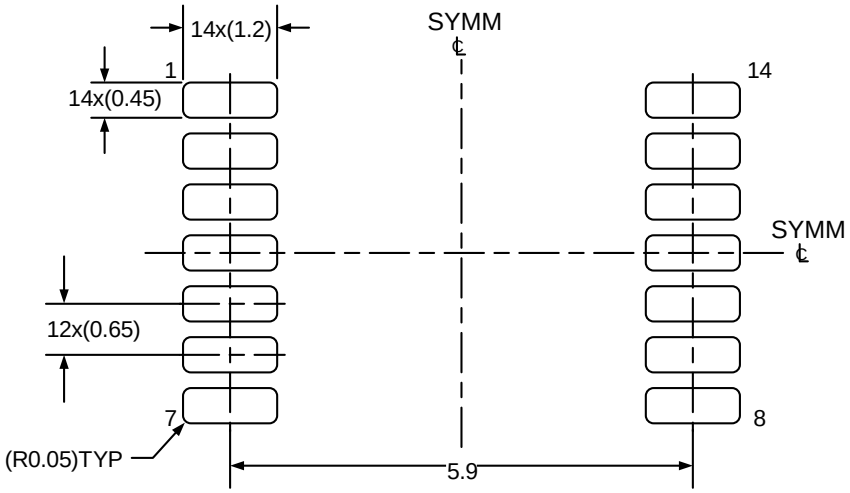
SOIC-14L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

TSSOP-14L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30AP321NNSTR-I01	SOT23-5L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP321NNDTR-I01	SC70-5L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP358NWLTR-I02	SOIC-8L	Green	Tape & Reel	4000	−40°C to +125°C
GD30AP358NWETR-I02	DFN2x2-8L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP358NWMTR-I02	MSOP-8L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP324NZLTR-I04	SOIC-14L	Green	Tape & Reel	2500	−40°C to +125°C
GD30AP324NZPTR-I04	TSSOP-14L	Green	Tape & Reel	3000	−40°C to +125°C
GD30AP324NLUTR-I04	QFN3x3-16L	Green	Tape & Reel	3000	−40°C to +125°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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